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or interconnect* or wir* or
damascene or dualdamascene)
and (ce or zr or la) and
```

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	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	259335	((metal or Ce or cerium or La or lanthanum or Zr or zirconium) adj oxide) or (CeO or LaO or ZrO) or ((Ce or Ce?sub$4 or La or La?sub$4 or Zr or Zr?sub$4) adj (O or O?sub$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 13:58	
12	BRS	L12	8423	1 with (cap or capping or passivat$4 or protect$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:04	
14	BRS	L14	7720	1 same (thermal$4 or anneal$4 or heat$6 or RTA or RTP) same (alloy$6 or diffus$6 or interdiffus$4 or migra$6 or immigra$6 or mov$6 or transform$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:01	
15	BRS	L15	15552	12 or 14	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:01	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
16	BRS	L16	5483	15 and (semiconductor or dualdamascene or damascene or interconnect$4 or multiwiring or metallizat$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:02	
17	BRS	L17	4349	16 and (cap or capping or passivat$4 or protect$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:02	
19	BRS	L19	3105	17 and (thermal$4 or anneal$4 or heat$6 or RTA or RTP)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:12	
21	BRS	L21	1770	19 and @ad<=20001218	USPAT; US-PGPUB	2004/09/09 14:13	
22	BRS	L22	1010	19 and @rlad<=20001218	USPAT; US-PGPUB	2004/09/09 14:13	
23	BRS	L23	2170	21 or 22	USPAT; US-PGPUB	2004/09/09 14:13	
24	BRS	L24	475	23 and (planariz$4 or polish$4 or CMP)	USPAT; US-PGPUB	2004/09/09 14:14	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	259335	((metal or Ce or cerium or La or lanthanum or Zr or zirconium) adj oxide) or (CeO or LaO or ZrO) or ((Ce or Ce?sub$4 or La or La?sub$4 or Zr or Zr?sub$4) adj (O or O?sub$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 13:58	
12	BRS	L12	8423	1 with (cap or capping or passivat$4 or protect$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:04	
14	BRS	L14	7720	1 same (thermal$4 or anneal$4 or heat$6 or RTA or RTP) same (alloy$6 or diffus$6 or interdiffus$4 or migra$6 or immigra$6 or mov$6 or transform$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:01	
15	BRS	L15	15552	12 or 14	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:01	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
16	BRS	L16	5483	15 and (semiconductor or dualdamascene or damascene or interconnect$4 or multiwiring or metallizat$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:02	
17	BRS	L17	4349	16 and (cap or capping or passivat$4 or protect$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:02	
19	BRS	L19	3105	17 and (thermal$4 or anneal$4 or heat$6 or RTA or RTP)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:05	
20	BRS	L20	149	17 and (thermal$4 or anneal$4 or heat$6 or RTA or RTP)	EPO; JPO; DERWENT; IBM_TDB	2004/09/09 14:06	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	259335	((metal or Ce or cerium or La or lanthanum or Zr or zirconium) adj oxide) or (CeO or LaO or ZrO) or ((Ce or Ce?sub$4 or La or La?sub$4 or Zr or Zr?sub$4) adj (O or O?sub$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 11:36	
2	IS&R	L2	19886	(438/622-688).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/09 11:36	
3	BRS	L3	2282	1 and 2	USPAT; US-PGPUB	2004/09/09 11:37	
4	BRS	L4	1866	3 and (thermal$4 or anneal$4 or heat$6 or RTA or RTP)	USPAT; US-PGPUB	2004/09/09 11:38	
5	BRS	L5	1232	4 and @ad<=20001218	USPAT; US-PGPUB	2004/09/09 11:38	
6	BRS	L6	496	4 and @rlad<=20001218	USPAT; US-PGPUB	2004/09/09 11:38	
7	BRS	L7	1427	5 or 6	USPAT; US-PGPUB	2004/09/09 11:38	
8	BRS	L8	31392	1 same (thermal$4 or anneal$4 or heat$6 or RTA or RTP)	USPAT; US-PGPUB	2004/09/09 11:38	
10	BRS	L10	330	7 and 8	USPAT; US-PGPUB	2004/09/09 11:38	

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     (FILE 'HOME' ENTERED AT 15:31:12 ON 09 SEP 2004)

     FILE 'REGISTRY' ENTERED AT 15:31:26 ON 09 SEP 2004
L1           349 S CE.O/MF OR CE O/ELF
L2           293 S LA.O/MF OR LA O/ELF
L3          1124 S O.ZR/MF OR O ZR/ELF

     FILE 'HCAPLUS' ENTERED AT 15:36:22 ON 09 SEP 2004
L11        36135 S L1 OR (CE OR CERIUM)(3N)OXID?
L12        51612 S L2 OR (LA OR LANTHANUM)(3N)OXID?
L13       108493 S L3 OR (ZR OR ZIRCONIUM)(3N)OXID?
L14        14139 S (L11 OR L12 OR L13) AND (ANNEAL? OR RTP OR RTA OR (HEAT OR TH
L15         1298 S L14 AND (CAP OR CAPING OR PASSIVAT? OR BARRIER? OR PROTECT?)
L16           23 S L15 AND (CAP OR CAPING)
L17         1275 S L15 NOT L16
L18         1275 S L17 AND (PASSIVAT? OR BARRIER? OR PROTECT?)
L19           47 S L18 AND PASSIVAT?
L20            3 S L19 AND BARRIER?
L21           44 S L19 NOT L20
L22            8 S L21 AND METAL?(3N)(OXID? OR CONDUCT?)
L23           36 S L21 NOT L22
L24           29 S L23 AND ANNEAL?
L25            2 S L24 AND (INTER()CONNECT? OR INTERCONNECT? OR METALIZAT? OR WI
L26           27 S L24 NOT L25
L27            0 S L26 AND (INTER()CONNECT? OR INTERCONNECT? OR METALIZAT? )
L28            0 S L16 AND (METALIZAT? OR METALLIZAT? OR METALLISAT? OR METALISA
L29            0 S L16 AND (WIRING OR WIRED)
L30         1448 S (L11 OR L12 OR L13) AND (INTER()CONNECT? OR INTERCONNECT? OR
L31          253 S L30 AND METAL?(3N)(OXID? OR CONDUCT?)
L32           31 S L31 AND (CAP OR CAPING OR PASSIVAT? OR BARRIER? OR PROTECT?)
L33           31 S L32 NOT L16,L19
L34            4 S L33 AND (ANNEAL? OR RTP OR RTA OR (HEAT? OR THERMAL?)(3N)(PRO
L35           27 S L33 NOT L34
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L25 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:391993 HCAPLUS
DN 134:360360
TI Polarization method for minimizing the effects of hydrogen damage on ferroelectric thin film capacitors which allows use of forming gas **annealing**
IN Sun, Shan; Traynor, Steven D.
PA Ramtron International Corporation, USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6238933	B1	20010529	US 1999-305949	19990506
PRAI US 1999-305949		19990506		

AB Ferroelec. switching properties are severely degraded in a H ambient atmospheric
By controlling the polarity of the capacitors in a ferroelec. memory during the manufacturing process, the amount of degradation can be significantly
reduced. After **metalization** of a ferroelec. memory wafer, all of the ferroelec. capacitors are poled in the same direction. The polarization vector is in a direction that helps to counteract H damage. A H gas **anneal** is subsequently performed to control underlying CMOS structures while maintaining ferroelec. elec. properties. The wafer is then **passivated** and tested.
RE.CNT 30 THERE ARE 30 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:52293 HCAPLUS
DN 128:174829
TI The hysteresis caused by interface trap and anomalous positive charge in Al/CeO2-SiO2/silicon capacitors
AU Roh, Yonghan; Kim, Kyunghae; Jung, Donggeun
CS Dep. Electronic Engineering, Sung Kyun Kwan Univ., Suwon, 440-746, S. Korea
SO Japanese Journal of Applied Physics, Part 2: Letters (1997), 36(12B), L1681-L1684
CODEN: JAPLD8; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB The authors report the hysteresis induced by two similar defects located at and near the SiO2-Si interface in the Al/CeO2-SiO2/Si capacitor. The authors find that the hysteresis are generated directly due to the presence of interface trap and anomalous pos. charge. Elec. characteristics of the hysteresis are, however, distinct and are strongly dependent on the type of defects. For example, the hysteresis caused by interface traps disappeared after **passivating** the Si dangling bonds by a post **metalization annealing**, while only a bias-temperature **annealing** causes the reduction of the hysteresis generated by anomalous pos. charge. The authors suggest the mechanisms of the hysteresis generation in the Al/CeO2-SiO2/Si capacitor.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

TOT

L34 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:108001 HCAPLUS
DN 140:342035
TI LaCrO3-based coatings on ferritic stainless steel for solid oxide fuel cell **interconnect** applications
AU Zhu, J. H.; Zhang, Y.; Basu, A.; Lu, Z. G.; Paranthaman, M.; Lee, D. F.; Payzant, E. A.
CS Department of Mechanical Engineering, Tennessee Technological University, Cookeville, TN, 38505, USA
SO Surface and Coatings Technology (2004), 177-178, 65-72
CODEN: SCTEEJ; ISSN: 0257-8972
PB Elsevier Science B.V.
DT Journal
LA English
AB A thin layer of doped lanthanum chromite on ferritic steel may act as a **protective** coating to mitigate the Cr volatility problems and facilitate the use of **metallic interconnect** in solid **oxide** fuel cells operated at intermediate temps. The LaCrO3 thin film was successfully synthesized on a ferritic stainless steel substrate by two approaches, i.e. reactive formation and sol-gel processing. The coating structures and surface morphologies were analyzed using x-ray diffraction and SEM. After isothermal oxidation at 850° for 100 h in air, the elec. resistance of the sol-gel coated samples remained very low, as compared to that of the uncoated sample after similar thermal exposure. The sol-gel coating also provided effective **protection** for the **interconnect** steel during oxidation of twelve 100-h cycles at 800° in air, whereas significant spallation and weight loss were observed for the uncoated steel. The two coating processes (i.e. reactive formation and sol-gel processing) were compared and their advantages and drawbacks were outlined.
RE.CNT 25 THERE ARE 25 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:913781 HCAPLUS
DN 136:122259
TI Investigations on chromium release from metallic **interconnect** materials for Solid Oxide Fuel Cell (SOFC) applications
AU Gindorf, Christian
CS Germany
SO Berichte des Forschungszentrums Juelich (2001), Juel-3853, i-vii, 1-101
CODEN: FJBEE5; ISSN: 0366-0885
DT Report
LA German
AB Metallic **interconnect** materials (chromium-based alloys and chromium-containing steels) form volatile chromium species under operating conditions of the Solid Oxide Fuel Cell. These volatile Cr(VI) species are reduced to solid Cr(III) compds. at the triple phase boundary cathode/electrolyte/oxidant after penetrating the cathode material, leading to a degradation of the electrochem. properties of the cell. In this work the vaporization of volatile chromium species was studied by the transpiration method. Transpiration expts. were carried out under equilibrium as well as non-equilibrium conditions. Equilibrium studies were carried out in air, using Cr2O3(s) (powder) at different water partial pressures (between 0.7

mbar and 0.3 bar) and temps. (between 400 °C and 950 °C). Thermodn. calcns. based on the measured temperature dependence yielded an enthalpy of reaction of ΔrH948 = 122.85 kJ/mol for the formation of the volatile chromium species CrO2(OH)2(g) (dominating in the vapor over Cr2O3(s) under these exptl. conditions). Transpiration expts. under non-equilibrium conditions were carried out at a water vapor pressure of p(H2O) = 0.02 bar at temps. of 850 °C and 950 °C. The chromium vaporization rate of metallic **interconnect** materials forming different oxide scales as well as the chromium vaporization of different coated alloy samples (perovskite coatings on Cr5FeIY2O3 and X10CrA118 substrates) were determined Perovskite coatings are used as a diffusion **barrier** against volatile chromium(VI) species vaporizing from the **interconnect** surface. In this work the chromium retention potential of vacuum plasma sprayed coatings (scale thickness 25-30 μm) was investigated by comparison of chromium transport rates of coated and uncoated **interconnect** samples. As a result of this expts. a chromium retention of more than 99% was found for **protective** perovskite coatings (e.g. La0.9Sr0.1CrO3) under cathodic operating conditions of the SOFC. Investigations of the scale morphol. of perovskite coatings revealed a time dependent densification process. Due to that densification process possible values of more than 99% were observed after different **annealing** times. The vaporization of volatile chromium(VI) species from coated **interconnect** specimens is caused by cracks and pores in the **protective** scale. This was confirmed by 53Cr tracer expts. with **protective** perovskite scales based on lanthanum chromite which were carried out to obtain chromium self diffusion coeffs. For the scale composition of La0.9Sr0.1CrO3 at a temperature of 1000 °C a chromium diffusion coefficient of 2.59·10-16 cm2/s was determined Considering a scale thickness of 30 μm, from this diffusion coefficient, a break through time of 550 yr can be calculated According to these results, grain boundary diffusion as well as bulk diffusion are too slow to compete with gas phase transport of chromium through the **protective** scale. Considering the results of this work it is possible to reduce the chromium deposition rate in the cathode by a factor of more than two orders of magnitude if the SOFC operating temperature is decreased by 100 °C from 950 °C to 850 °C and if proper substrate/coating combinations are used.

RE.CNT 114 THERE ARE 114 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:560035 HCAPLUS
DN 135:115627
TI Semiconductor capacitor fabrication method preventing electrode oxidation during dielectric film **annealing**
IN Joo, Jae Hyun; Park, Jong Bum
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6268258	B1	20010731	US 2000-558213	20000426
PRAI	KR 1999-42405	A	19991001		

AB A method is presented for fabricating a capacitor in a semiconductor device, in which oxidization of upper and lower electrodes and **wiring** films is prevented during **annealing** a capacitor dielec. film for improving device characteristics, the capacitor having a lower electrode, a dielec. film formed on a surface of the lower electrode, and an upper electrode formed on the dielec. film, the method including the steps of: (1) forming the dielec. film of at least one oxide selected from a group of **oxides** of Pb, **Zr**, Ta, Ba , Sr , and Ti ; (2) forming the upper electrode and the lower electrode of the capacitor with a metal having a standard Gibbs free energy greater than an **oxide metal** of the dielec. film; and (3) **annealing** to crystallize the dielec. film in an atmospheric of which partial pressure ratio of P(H2O)/P(H2) is in the range 10-20-100.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:533421 HCAPLUS
DN 131:202169
TI New cost-effective ceramic oxide phases used as **protective** coatings for chromium-based **interconnects**
AU Batawi, E.; Plas, A.; Straub, W.; Honegger, K.; Diethelm, R.
CS Sulzer Innotec Ltd., Div., Winterthur, CH-8401, Switz.
SO Proceedings - Electrochemical Society (1999), 99-19(Solid Oxide Fuel Cells (SOFC VI)), 767-773
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB Stability of high-temperature solid oxide fuel cells (SOFC's), fitted with metallic **interconnects** can only be achieved when **protective** coatings are deposited on all surfaces prone to chromium oxide formation. Thermally sprayed substituted lanthanum manganites have proven to be effective in restricting the evaporation of chromium during service from these surfaces. The dense coating hinders transport of chromium species, both in the solid and gaseous phase, eliminating any performance degradation that may be caused by condensation of chromia in and on the cathode. Sulzer HEXIS Ltd. has successfully used this method in extended endurance testing of stacks and systems. Unfortunately however, because of the large quantities of material required to coat the **interconnects** and the high cost of the raw materials that enter the composition of the coating, the estimated cost of this coating is significantly higher than what can be allowed for market entry. A new family of perovskites, rich in alkaline earth elements and containing little or no lanthanum, were evaluated. Compns. such as Sr1-xLaxMnO3, Ca1-xLaxMnO3 and Ca1-xYxMnO3 were evaluated for their thermal expansion, high temperature conductivity and phase stability. Thermal spraying trials were carried out on chromium-based alloys and the contact resistance of the coated samples was measured.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 1 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:428876 HCAPLUS
DN 140:427623
TI Electric connection for electrically conductive ceramic sealing jaws
IN Selberg, Hans; Ingvert, Claes; Boeckerman, Bjoern; Nilsson, Tommy
PA Tetra Laval Holdings & Finance S.A., Switz.
SO PCT Int. Appl., 18 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2004043877	A1	20040527	WO 2003-SE1735	20031111
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD				
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
SE 2002003367	A	20040515	SE 2002-3367	20021114
PRAI SE 2002-3367	A	20021114		

AB Elec. connection for elec. conductive ceramic parts (such as sealing jaws) are manufactured by uniting a first elec. conductor with a portion of the elec. conductive ceramics (such as TiB and SiC) using a foil which has metalized the portion of the elec. conductive ceramics and fused together the portion with the elec. conductor.

L35 ANSWER 2 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:428555 HCAPLUS
DN 140:432521
TI Surface **barriers** for copper and silver **interconnects** produced by a **damascene** process
IN Farrar, Paul A.
PA Micron Technology, Inc., USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6740392	B1	20040525	US 2003-414147	20030415
PRAI US 2003-414147		20030415		

AB The present invention relates to a method of fabricating a **barrier** layer and, more particularly, to a method of fabricating a **barrier** layer on a top surface of metal in **damascene** structures utilizing ion implantation. A semiconductor device structure having a **barrier** layer comprising a conductive portion and a nonconductive portion is disclosed. The **conductive** portion includes a **metal** nitride compound and the non-**conductive** portion

includes a **metal oxide**, **metal** oxynitride, **metal** carbide, or metal carbonitride compound A method of forming the semiconductor device structure is also disclosed. The method comprises forming a **barrier** layer over a **metalization** layer and a dielec. layer in the semiconductor device structure. The **barrier** layer is formed by depositing a thin, metal layer over the **metalization** layer and the dielec. layer. The metal layer is exposed to a N2 atmospheric and the N2 reacts with portions of the metal layer over the **metalization** layer to form a **conductive**, **metal** nitride portion of the **barrier** layer. Portions of the metal layer over the dielec. layer react with C or O in the dielec. layer to produce a non-conductive portion of the **barrier** layer.

RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 3 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:310789 HCAPLUS
DN 140:348890
TI Ferroelectric capacitor memory device fabrication method
IN Lung, Hsiang-Lan
PA Macronix International Co., Ltd., Taiwan
SO U.S. Pat. Appl. Publ., 13 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2004072407	A1	20040415	US 2002-270997	20021015
PRAI US 2002-270997		20021015		

AB A ferroelec. capacitor memory device is fabricated by forming a substrate including integrated circuitry with an **interconnect** layer and pass transistors. First capacitor electrodes are formed on the substrate and are connected to an associated pass transistor through the **interconnect** layer. A ferroelec. dielec. layer, formed on the 1st capacitor electrodes, is patterned to expose portions of the 1st capacitor electrodes to form a contact opening and a pad region. A 2nd capacitor electrode is formed over the patterned ferroelec. layer to create a via within said contact opening, said via extending to said 1st capacitor electrode. A conductive layer is formed upon the 2nd capacitor electrode. The conductive layer is patterned to form a plate line, said via connecting the 1st capacitor electrode to said plate line. The substrate forming step may be carried out so that the pass transistors comprise sources, drains and gates and the integrated circuitry comprises complementary **metal oxide** semiconductor (CMOS) circuitry comprising word lines, bit lines **interconnect** metal lines and contact plugs.

L35 ANSWER 4 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:231113 HCAPLUS
DN 141:97145
TI Review of recent progress in atomic layer deposition (ALD) of materials for micro- and nano-electronics
AU Gordon, Roy G.
CS Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA, 02138, USA
SO Polymeric Materials Science and Engineering (2004), 90, 726-728

CODEN: PMSEDG; ISSN: 0743-0515
PB American Chemical Society
DT Journal; General Review; (computer optical disk)
LA English
AB A review. The authors review processes that the authors discovered recently for ALD of transition metals, **metal** nitrides and **metal oxides**. Successful ALD requires pairs of precursors with high but self-limiting reactivity with surfaces prepared by the complementary co-reactant, along with high thermal stability, sufficient volatility and non-etching behavior toward substrates and the deposited films. New precursor pairs meeting all of these demanding requirements were found for depositing the transition metals iron, cobalt, nickel and copper, their oxides, tungsten nitride, silicon dioxide, and **oxides** of hafnium, **zirconium**, **lanthanum**, praseodymium, tantalum, and bismuth. The metal deposition may be applicable to **interconnects** and to magnetic devices. Tungsten nitride is an excellent diffusion **barrier** at nanometer thicknesses. The silica deposition is suitable for filling isolation trenches in microelectronics. The substrate temps. are low enough so that applications of high-quality high-k dielecs. are possible to temperature sensitive substrates, such as carbon nano-tube transistors and photo-resist patterning by lift-off.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 5 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:228571 HCAPLUS
TI Review of recent progress in atomic layer deposition (ALD) of materials for micro- and nano-electronics
AU Gordon, Roy G.
CS Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA, 02138, USA
SO Abstracts of Papers, 227th ACS National Meeting, Anaheim, CA, United States, March 28-April 1, 2004 (2004), PMSE-417 Publisher: American Chemical Society, Washington, D. C.
CODEN: 69FGKM
DT Conference; Meeting Abstract
LA English
AB We review processes that we discovered recently for ALD of transition metals, **metal** nitrides and **metal oxides**. Successful ALD requires pairs of precursors with high but self-limiting reactivity with surfaces prepared by the complementary co-reactant, along with high thermal stability, sufficient volatility and non-etching behavior toward substrates and the deposited films. New precursor pairs meeting all of these demanding requirements were found for depositing the transition metals iron, cobalt, nickel and copper, their oxides, tungsten nitride, silicon dioxide, and **oxides** of hafnium, **zirconium**, **lanthanum**, praseodymium, tantalum, and bismuth. The metal deposition may be applicable to **interconnects** and to magnetic devices. Tungsten nitride is an excellent diffusion **barrier** at nanometer thicknesses. The silica deposition is suitable for filling isolation trenches in microelectronics. The substrate temps. are low enough so that applications of high-quality high-k dielecs. are possible to temperature sensitive substrates, such as carbon nano-tube transistors and photo-resist patterning by liftoff.

L35 ANSWER 6 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:928077 HCAPLUS
DN 140:184588
TI The effect of **protective** layers formed by electrophoretic deposition on **oxidation** and performance of **metallic interconnects**
AU Yoo, Yeong; Dauga, Marc
CS Institute for Chemical Process and Environmental Technology, National Research Council of Canada, Ottawa, ON, K1A 0R6, Can.
SO Proceedings - Electrochemical Society (2001), 2001-16(Solid Oxide Fuel Cells VII), 837-846
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB A decrease in cell operation temperature to the intermediate temperature range of 600-750° allows the use of cheaper and more **conductive metallic interconnect** materials instead of ceramics. However, the **oxide** scale on the **metal** surface has low electronic conductivity, and vaporization of chromia-containing oxide scale can cause degradation of cathode performance. To reduce degradation of cell performance that may be caused by the solid or gaseous phase reaction of chromium species, an effective **protective** layer should be developed. The electrophoretic deposition (EPD) process and the compns. of **protective** layers on chromium containing Fe or Ni based alloys such as ferritic stainless steels were studied. The growth rate of the oxide scale was determined by weight gain, before and after making deposits of **protective** layers on the alloys. The microstructure and contact resistance were evaluated. Uniform and dense depositions of perovskite powders on the stainless steels were achieved by electrophoretic deposition to improve the oxidation behavior and contact resistance of the metallic **interconnects** in the intermediate temperature solid oxide fuel cells (SOFCs).
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 7 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:510045 HCAPLUS
DN 139:45341
TI Electronic component comprising an integrated circuit and a planar micro capacitor
IN Girardie, Lionel
PA Memscap, Fr.
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 5

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1324376	A1	20030702	EP 2002-356255	20021210
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR, BG, CZ, EE, SK				
FR 2834387	A1	20030704	FR 2001-17069	20011231
FR 2834387	B1	20040227		

L16 ANSWER 1 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:633202 HCAPLUS
DN 141:165919
TI Integration method to enhance p+ gate activation
IN Guo, Jyh Chyurn
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2004152253	A1	20040805	US 2003-358632	20030205
PRAI US 2003-358632		20030205		

AB A new process integration method is described to form heavily doped p + source and drain regions in a CMOS device. After defining the p- and n-well regions on a semiconductor substrate, gate SiO2 is deposited and nitrided in a N-containing atmospheric Poly-Si is then deposited and the two NMOS and PMOS gates are formed. For the p+ doping of the poly-Si gate and S/D regions around the PMOS gate, B+ ions are then implanted. **Cap** dielec. layer comprising SiO2 is then deposited, followed by dopant activation with high temperature rapid thermal **annealing**. The **cap** dielec. layer is then used as resist **protective** film; it is removed from those areas of the chip that would require formation of elec. contacts. Silicide elec. contacts are then formed in these areas.

L16 ANSWER 2 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:607989 HCAPLUS
TI Characteristics of **Ce-Zr** mixed **oxide** films as buffer layer by controlling composition
AU Lee, H. Y.; Kim, S. I.; Lee, Y. C.; Hong, Y. P.; Ko, K. H.
CS Ajou University, Wonchon-dong Paldal-gu Suwon, S. Korea
SO IEEE Transactions on Applied Superconductivity (2003), 13(2, Pt. 3), 2665-2668
CODEN: ITASE9; ISSN: 1051-8223
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB YSZ films have been widely used as buffer layers for high Tc superconductor. However, it is necessary to investigate and develop another buffer layer with suitable, simple, and neat processing. Films of **Ce-Zr** mixed **oxide** were deposited by rf and do magnetron co-sputtering. In sputtering process, do power of Zr was fixed in 200 W while rf power of Ce was varied with 30 W, 50 W, 100 W, resp. As-deposited (CexZr1-x)O2 films were crystallized without post **annealing**. It was confirmed that the composition of the films could be controlled with controlling rf power of Ce target. The Φ scan of XRD showed that all (CexZr1-x)O2 films were (200) c-axis oriented. Three consecutive magnetron sputtering procedure for seed, CZO and **cap** layer for HTSC films using Ce, Zr and CeO2 target were carried out on the Si(100) and Ni substrate successfully. It is suggested that sputtered and c-axis oriented (CexZr1-x)O2 films can be a potential candidate to replacing YSZ buffer layer.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 3 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:231934 HCAPLUS
TI Calcium phosphates and glass composite coatings on zirconia for enhanced biocompatibility
AU Kim, Hae-Won; Georgiou, George; Knowles, Jonathan C.; Koh, Young-Hag; Kim, Hyoun-Ee
CS Eastman Dental Institute, Biomaterials and Tissue Engineering, University College London, London, WC1X 8LD, UK
SO Biomaterials (2004), 25(18), 4203-4213
CODEN: BIMADU; ISSN: 0142-9612
PB Elsevier Science Ltd.
DT Journal
LA English
AB Calcium phosphates (**CaP**) and phosphate-based glass (P-glass, xCaO-(0.55-x)Na2O-0.45P2O5 composition) composite coatings were obtained on a strong ZrO2 to improve biocompatibility, the mech. strength and biol. activity. Hydroxyapatite (HA) and P-glass mixed powder slurries were coated on the ZrO2 substrate, and subsequently **heat-treated** to obtain **CaP**- and P-glass composite coatings. The effects of glass composition (x=0.3, 0.4, 0.5 mol), mixing ratio of glass to HA (30%, 40%, 50% wt/wt), and **heat treatment** temperature (800°, 900°, 1000°) on the coating properties were investigated. After **heat treatment**, addnl. calcium phosphates, i.e., dicalcium phosphate (DCP) and tricalcium phosphate (TCP), were crystallized, resulting in the formation of triphasic calcium phosphates (HA-TCP-DCP) surrounded by a glass phase. The relative amts. of the crystalline phases varied with coating variables. The higher **heat treatment** temperature and glass amount, and the lower CaO content in the glass composition rendered the composite coatings to retain the higher amts. of TCP and DCP while the initial HA decreased. These appearance of addnl. crystalline phases and reduction of HA amount were attributed to the combined effects, i.e., the melting-crystallization of P-glass and the reaction between glass liquid phase and HA powder during **thermal treatment**. As a result of the glass phase in the composite coatings, their microstructures became much denser when compared to the pure HA coating. In particular, a completely dense structure was obtained at coating conditions with large amount of glass addition (50%) at the glass composition of lower CaO content (0.3 mol CaO), and the following **heat treatment** above 800° for 2 h. As a result, the adhesion strengths of the composite coating layers were significantly improved when compared to the pure HA coating. The highest strength of the composite coating was .apprx.40 MPa, an improvement of .apprx.80% with respect to the pure HA coating. The composite coatings showed much higher dissoln. rates than the pure HA coating due to the newly formed crystallines (TCP and DCP) and the remaining glass phase. The osteoblast-like cells grew and spread actively on the composite coating samples. The proliferation nos. and alkaline phosphate (ALP) activities of the cells on the composite coatings were improved by .apprx.30-40% when compared to Thermanox control and ZrO2 substrate, and were comparable to the pure HA coating. These findings suggested that the **CaP** and P-glass composites are potentially useful for hard tissue coating system, due to their morphol. and mech. integrity, enhanced bioactivity, and favorable responses to the osteoblast-like cells.

RE.CNT 36 THERE ARE 36 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 4 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:944302 HCAPLUS
DN 140:244323
TI MOD approach for the growth of epitaxial CeO2 buffer layers on biaxially textured Ni-W substrates for YBCO coated conductors
AU Bhuiyan, M. S.; Paranthaman, M.; Sathyamurthy, S.; Aytug, T.; Kang, S.; Lee, D. F.; Goyal, A.; Payzant, E. A.; Salama, K.
CS Oak Ridge National Laboratory, Oak Ridge, TN, 37831, USA
SO Superconductor Science and Technology (2003), 16(11), 1305-1309
CODEN: SUSTEF; ISSN: 0953-2048
PB Institute of Physics Publishing
DT Journal
LA English
AB We have grown epitaxial CeO2 buffer layers on biaxially textured Ni-W substrates for YBCO coated conductors using a newly developed metalorg. decomposition (MOD) approach. Precursor solution of 0.25 M concentration was spin coated on short samples of Ni-3 at%W (Ni-W) substrates and **heat-treated** at 1100°C in a gas mixture of Ar-4%H2 for 15 min. Detailed x-ray studies indicate that CeO2 films have good out-of-plane and in-plane textures with full-width-half-maximum values of 5.8° and 7.5°, resp. High temperature in situ XRD studies show that the nucleation of CeO2 films starts at 600°C and the growth completes within 5 min when heated at 1100°C. SEM and AFM investigations of CeO2 films reveal a fairly dense microstructure without cracks and porosity. Highly textured YSZ **barrier** layers and CeO2 **cap** layers were deposited on MOD CeO2-buffered Ni-W substrates using rf-magnetron sputtering. Pulsed laser deposition (PLD) was used to grow YBCO films on these substrates. A critical current, Jc, of about 1.5 MA cm-2 at 77 K and self-field was obtained on YBCO (PLD)/CeO2 (sputtered)/YSZ (sputtered)/CeO2 (spin-coated)/Ni-W.
RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 5 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:394762 HCAPLUS
DN 140:169508
TI Corundum Ceramics for Medical Purposes
AU Lukin, E. S.; Tarasova, S. V.; Popova, N. A.; Makarov, N. A.
CS D. I. Mendeleev Russian Chemical Engineering University, Moscow, Russia
SO Glass and Ceramics (Translation of Steklo i Keramika) (2003), 60(1-2), 26-29
CODEN: GLCEAV; ISSN: 0361-7610
PB Kluwer Academic/Consultants Bureau
DT Journal
LA English
AB The possibilities of using various kinds of aluminum oxide materials, modifying additives, and temporary technol. binders for making bioinert ceramics based on aluminum oxide are considered. Regimes for **heat treatment** of intermediate pieces are developed. A ceramic material with a mean d. of 4.01 g/cm3, 3-point bending strength 380 ±20 MPa, a size of corundum crystal equal to 4 - 6 μm, and zero open porosity is obtained, which can be used in endoprostheses **caps** for coxofemoral joints.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 6 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:86738 HCAPLUS
DN 138:361108
TI Surface preparation and interfacial stability of high-k dielectrics deposited by atomic layer chemical vapor deposition
AU Tsai, W.; Carter, R. J.; Nohira, H.; Caymax, M.; Conard, T.; Cosnier, V.; DeGendt, S.; Heyns, M.; Petry, J.; Richard, O.; Vandervorst, W.; Young, E.; Zhao, C.; Maes, J.; Tuominen, M.; Schulte, W. H.; Garfunkel, E.; Gustafsson, T.
CS International Sematech/IMEC, Louvain, B-3001, Belg.
SO Microelectronic Engineering (2003), 65(3), 259-272
CODEN: MIENEF; ISSN: 0167-9317
PB Elsevier Science B.V.
DT Journal
LA English
AB The effects of various interface prepns. on atomic layer chemical vapor deposition (ALCVD) deposited Al2O3 and ZrO2 dielecs. properties were investigated by XPS, attenuated total reflection Fourier transform IR spectroscopy (ATR-FTIR), medium energy ion scattering (MEIS) and transmission electron microscopy (TEM). H-terminated Si, SiO2 and SiOxNy surfaces were used as substrates upon which the dielec. was deposited. Thermal **annealing** of SiO2 in NH3 forms an oxynitride; subsequent deposition of a ZrO2/Al2O3 bi-layer stack resulted in a capacitor structure with an equivalent oxide thickness (EOT) of .apprx.0.8 nm and a leakage current of 3+10-4 A/cm2 at -1+Vfb. This is in contrast to capacitor structures grown on H-terminated Si where high leakage was found. The growth of addnl. interfacial SiO2 during processing, a critical problem in nano-electronic device applications, is temperature dependent with ZrO2 exhibiting a higher oxygen permeability than Al2O3. Use of a polysilicon **cap** was shown to be effective at blocking oxygen absorption and transport through the high-k dielecs., with stability up to 1100 °C.
RE.CNT 26 THERE ARE 26 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 7 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:886645 HCAPLUS
DN 137:361571
TI Dielectric memory devices and fabrication of devices thereof
IN Nagasawa, Yutaka; Nagata, Masaya; Ishihara, Kazunari; Matsu, Yoshiyuki
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 15 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002334969	A2	20021122	JP 2001-136199	20010507
PRAI	JP 2001-136199		20010507		

AB The title devices have an electrode/dielec./electrode laminated capacitor and a **cap** layer to **protect** the capacitor electrode in shape during **annealing** for characteristic controlling. The **cap** layer is made from Al oxide, Al nitride, Al oxynitride, Ta

oxide, Ta oxynitride, Ti **oxide**, or **Zr oxide**.
The dielec. layer may be made from ferroelec. or high dielec. materials.
The **cap** layer **protects** the upper capacitor electrode
against aggregation otherwise caused by **annealing**.

L16 ANSWER 8 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:638951 HCAPLUS
DN 137:360957
TI Electrical characteristics of ZrO2 gate dielectric deposited on ultrathin silicon capping layer for SiGe metal-oxide-semiconductor device applications
AU Choi, Sangmoo; Jeon, Sanghun; Hwang, Hyunsang; Song, Young J.; Lim, Jung-Wook; Shim, Kyu-Hwan; Park, Kyung Wan
CS Department of Materials Science and Engineering, Kwangju Institute of Science and Technology, Kwangju, 500-712, S. Korea
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2002), 41(8), 5129-5130
CODEN: JAPNDE
PB Japan Society of Applied Physics
DT Journal
LA English
AB The elec. characteristics of ZrO2 were studied relative to its use in SiGe metal-oxide-semiconductor (MOS) gate dielec. applications. Compared to ZrO2 directly deposited on SiGe, ZrO2, when deposited on a silicon capping layer shows a significant improvement in elec. characteristics such as low leakage current, negligible hysteresis, less fixed charge d. and a lower interface state d. (Dit) after low-temperature wet vapor **annealing**. The improvement in the elec. characteristics of ZrO2, with a silicon capping layer can be attributed to the negligible Ge segregation and surface roughness at the interface. Based on an Auger electron spectroscopy (AES) depth profile of Ge, the authors were able to confirm that Ge is segregated at the interface.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 9 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:543352 HCAPLUS
DN 137:302793
TI Interface reactions in ZrO2 based gate dielectric stacks
AU Gribelyuk, M. A.; Callegari, A.; Gusev, E. P.; Copel, M.; Buchanan, D. A.
CS IBM Microelectronics Division, Hopewell Junction, NY, 12533, USA
SO Journal of Applied Physics (2002), 92(3), 1232-1237
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB Interface reactions in Si/SiOx(Ny)/ZrO2 and Si/SiOx(Ny)/ZrO2/poly-Si gate stacks have been studied by HRTEM microscopy. In the case of an uncapped stack, ZrSi and ZrSi2 phases form during an ultrahigh vacuum **anneal** at temps. above 900°. Both phases show an island-type growth with an epitaxial relation with Si (100). Gate dielec. stacks with a poly-Si **cap** are found to be thermally unstable at T = 1000°, so that the reaction is initiated at the ZrO2/poly-Si interface. Here, a different reaction mechanism is identified, which involves the reduction of ZrO2 and the growth of a bottom interfacial layer between ZrOx and Si. Replacement of the bottom SiO2 layer by an ultrathin Si oxinitride does not completely suppress these interfacial reactions at

T 1000°. The authors suggest that control of the poly-Si/ZrO2 interfacial reactions may be an important factor in modifying the thermal stability of a stack. These results shed a new light on understanding the material challenges involved in the integration of ZrO2 for the next generation of CMOS technologies.
RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 10 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:547436 HCAPLUS
DN 135:260943
TI Process-microstructure-property relationships in controlled atmosphere plasma spraying (**CAPS**) of ceramics
AU Beauvais, S.; Guipont, V.; Borit, F.; Jeandin, M.; Espanol, M.; Khor, K. A.; Robisson, A.; Saenger, R.
CS Ecole Des Mines de Paris, Evry, Fr.
SO Thermal Spray 2001: New Surfaces for a New Millennium, Proceedings of the International Thermal Spray Conference, Singapore, Singapore, May 28-30, 2001 (2001), 479-486. Editor(s): Berndt, Christopher C.; Khor, Khiam A.; Lugscheider, Erich F. Publisher: ASM International, Materials Park, Ohio. CODEN: 69BOKQ
DT Conference
LA English
AB **Thermal** plasma spray **processes** with their various operating parameters can be considered as flexible technique to carry out appropriate ceramic coatings. This work deals with plasma spraying of several ceramics powders (hydroxyapatite (HA), Al2O3-TiO2, Al2O3, ZrO2-Y2O3 (YSZ) and Cr2O3) with suitable parameters using a **CAPS** system ("Controlled Atmospheric Plasma Spraying"). The HPPS (High Pressure Plasma Spraying), APS (Air Plasma Spraying) and IPS (Inert Plasma Spraying) modes were applied in order to obtain the suitable microstructure. The microstructures and phase compns. allowed to establish that surrounding high-pressure in the **CAPS** chamber is leading to a good heating of the powder and a good quality for the coatings.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 11 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:681032 HCAPLUS
DN 134:12125
TI Fabrication of (Hg,Re)-1212 thin films with flat surface on various substrates
AU Inoue, Nobuyoshi; Sugano, Tsuyoshi; Tsukamoto, Akira; Wu, Xiao-Jing; Utagawa, Tadashi; Adachi, Seiji; Tanabe, Keiichi
CS SRL-ISTEC, Tokyo, 135-0062, Japan
SO Advances in Superconductivity XII, Proceedings of the International Symposium on Superconductivity (ISS'99), 12th, Morioka, Japan, Oct. 17-19, 1999 (2000), Meeting Date 1999, 897-899. Editor(s): Yamashita, Tsutomu; Tanabe, Kei-ichi. Publisher: Springer-Verlag Tokyo, Tokyo, Japan. CODEN: 69AJQC
DT Conference
LA English
AB The authors improved the surface morphol. of (Hg,Re)-1212 thin films on STO (100), LSAT(100) and LAO(100) substrates, and achieved a high value of the critical c.d. Jc on STO substrates. A 100-nm-thick Re0.1Ba2CaCu2O2 precursor film with an HgO **protective cap** layer was

deposited on each substrate by pulsed laser deposition and subsequently **annealed** under an appropriate Hg vapor pressure in an evacuated quartz tube. The thickness of the obtained films was .apprx.75 nm. Large pinholes and out-growths were not conspicuously observed on the surface, indicating that homogeneous epitaxial growth was realized by employing rather thin Re0.1Ba2CaCu2O2 precursor films. As-fabricated films exhibited Tc0 = 109-117 K. The Jc values at 77 K in a self-field were 1.0 + 107, 4.5 + 106 and 2.7 + 106 A/cm2 for STO, LSAT and LAO substrates, resp.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 12 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:449802 HCAPLUS
DN 133:186100
TI Epitaxial growth of La2Zr2O7 thin films on rolled Ni-substrates by sol-gel process for high Tc superconducting tapes
AU Chirayil, T. G.; Paranthaman, M.; Beach, D. B.; Lee, D. F.; Goyal, A.; Williams, R. K.; Cui, X.; Kroeger, D. M.; Feenstra, R.; Verebelyi, D. T.; Christen, D. K.
CS Chemical and Analytical Sciences Division, Oak Ridge National Laboratory, Oak Ridge, TN, 37831-6100, USA
SO Physica C: Superconductivity and Its Applications (Amsterdam) (2000), 336(1&2), 63-69
CODEN: PHYCE6; ISSN: 0921-4534
PB Elsevier Science B.V.
DT Journal
LA English
AB A solution process was used to grow epitaxial La2Zr2O7 (LZO) buffer layers on roll-textured Ni (100) substrates to produce YBa2Cu3O7-δ (YBCO)-coated conductors. The LZO precursor solution was prepared by an all alkoxide sol-gel route using mixed metal methoxyethoxides in 2-methoxyethanol. The partially hydrolyzed solution was either spin-coated or dip-coated onto the textured Ni substrates. The amorphous thin film was then **heat treated** at 1150°C under (96%)Ar/(4%)H2 atmosphere for 1 h. X-ray diffraction (XRD) of the buffer layer indicated a strong c-axis orientation on the Ni (100) substrate. The LZO (222) pole figure revealed a single cube-on-cube texture. SEM images of the LZO buffer layer showed a dense microstructure without cracks. The YBCO deposited on the sol-gel LZO-buffered Ni substrates with sputtered YSZ and CeO2 top layers had a critical c.d. of 480,000 A/cm2 at 77 K and self-field.

RE.CNT 34 THERE ARE 34 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 13 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:267402 HCAPLUS
DN 132:295089
TI Antifouling and antibacterial fiber structure with good washfastness and deodorant property
IN Ezawa, Rumi; Honda, Hidenobu; Saito, Kimiichi
PA Toray Industries, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000119956	A2	20000425	JP 1998-287986	19981009
PRAI	JP 1998-287986		19981009		

AB The structure such as curtain, etc., comprises on the fiber surface a noncrystn. Ti peroxide particle layer, a zeolite layer, and/or an alkyl silicate layer and further on the surface a hydrophilic resin or a fluoro resin and a photocatalyst semiconductor. Treating Ti(OH)4 with aqueous H2O2, soaking a polyester cloth in the solution, drying at 120°, soaking with a solution containing 0.1% (ST-01) and 10% ethylene glycol-dimethyl terephthalate-polyethylene glycol copolymer, drying and **heat treatment** gave an antifouling cloth, useful for uniforms.

L16 ANSWER 14 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:742772 HCAPLUS
DN 132:72501
TI The magnetism of a buried La0.7Sr0.3MnO3 interface
AU Stadler, S.; Idzerda, Y. U.; Chen, Z.; Ogale, S. B.; Venkatesan, T.
CS Material Physics Branch, Naval Research Laboratory, Washington, DC, 20375, USA
SO Applied Physics Letters (1999), 75(21), 3384-3386
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB Using x-ray absorption spectroscopy (XAS) and x-ray MCD (XMCD) techniques, we have studied the electronic structure and magnetic properties of La0.7Sr0.3MnO3 (LSMO) as a function of YBa2Cu3O7-δ (YBCO) **cap** layer thickness. The Mn L2,3 XAS and XMCD data clearly show that the magnetic properties and electronic structure of the LSMO are adversely affected by the YBCO overlayer, owing to cation displacement/exchange that effectively reduces the La atom concentration in the LSMO near the YBCO/LSMO interface.
RE.CNT 31 THERE ARE 31 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 15 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:700998 HCAPLUS
DN 129:321231
TI Tooth replacement, especially crown or bridge, and method for its production
IN Nitoumbi, Blanchard; Murano, Donato
PA Castolin S. A., Switz.
SO Ger. Offen., 6 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19714759	A1	19981015	DE 1997-19714759	19970410
PRAI	DE 1997-19714759		19970410		

AB A tooth replacement which fits over a tooth stump comprises a metallic inner **cap** (preferably of Ti) which bears a thermally sprayed outer ceramic coating 40-200 μm thick, over which is placed a ceramic outer **cap**. Bonding of the thermally sprayed layer with the inner and outer **caps** is effected by sintering at

650-850°.

L16 ANSWER 16 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:661544 HCAPLUS
DN 129:264228
TI Hermetically joined ceramic components, and method for joining the components
IN Atherton, Glyn; Heavens, Stephen Nicholas; Jones, Ivor Wynn; Pender, John Angus
PA IONOTEC Ltd., UK
SO PCT Int. Appl., 30 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9842636	A1	19981001	WO 1998-GB920	19980326
W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG				
AU 9868438	A1	19981020	AU 1998-68438	19980326
PRAI GB 1997-6299		19970326		
WO 1998-GB920		19980326		

AB The joined components comprise a ceramic-glass joint formed by injecting between the joining surfaces a suspension comprising a mixture consisting of 50-90 weight% glass powder and balance ceramic powder, and a low-viscosity liquid in an amount of 20-60 weight% (based on the suspension), and drying the suspension, and **heat-treating** the joint. This method is suitable for bonding solid electrolyte ionically conductive ceramic tubes to an insulating ceramic header plate, e.g., in high-temperature Na batteries and thermoelec. energy conversion devices. The low-viscosity suspension results in the absence of voids and unwanted residues in the joint. A mixture consisting of 1 kg Al_2O_3 powder (mean particle size 3 μm) and 2 kg glass powder (SiO_2 46, B_2O_3 25, Al_2O_3 10, Na_2O 4, CaO 3, SrO 6, and BaO 6 weight%) was used in the preparation of a suspension containing the 1 kg powder mixture, 10 g polyethyleneglycol 1540, Rubini dye 1 mL, and deionized water 450 mL. The suspension was used for bonding a β-Al_2O_3 tube (outside diameter 20, wall thickness 1 mm) to an α-Al_2O_3 ring **cap** (inside diameter 20.5 mm) by heating the assembly to 1000°. The resulting bond was leak-tight to He even though the joint contained 10-20% voids.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 17 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:664611 HCAPLUS
DN 123:63318
TI Mechanical stresses during solid state amorphization of Zr/Co multilayers
AU Moske, M.; Samwer, K.
CS Inst. Phys., Univ. Augsburg, Augsburg, D-86135, Germany

SO Materials Research Society Symposium Proceedings (1995), 356(Thin Films: Stresses and Mechanical Properties V), 27-32
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB Thin film structures of crystalline Zr and Co, deposited in ultra-high vacuum, are investigated by bending beam technique and by x-ray diffraction. During isothermal **annealing** and interdiffusion reaction of the thin film double layer and multilayer packages, large compressive stresses are generated while an amorphous ZrCo-phase is formed. This can, at first hand, be understood in terms of the Kirkendall effect where Co atoms, as the main moving species, lead to a volume increase of the film beyond the Co interface. The observed change in Zr lattice spacing in accordance with the evolution of mech. stress indicates that the compressive stress is built up particularly within the Zr layer due to the solution of Co in Zr grains during the initial amorphization reaction. Film structures, having Co already present in the crystalline Zr layer after film deposition, show a decrease in reaction kinetics combined with a lower stress level, indicating that the interdiffusion reaction is dependent on the stress state in the Zr grains. At late stages of **annealing** in high vacuum a sudden increase of addnl. compressive stress is observed, which could be attributed to the **oxidn.** of **Zr**, very likely due to the formation of diffusion paths for oxygen through the Co (**cap**-) layer (Kirkendall voids). Such oxidation behavior was not observed with samples measured in situ in UHV directly after film deposition.

L16 ANSWER 18 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:287737 HCAPLUS
DN 120:287737
TI Crystallization of ferroelectric film
IN Ishihara, Kazuya; Oonishi, Shigeo
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05206382	A2	19930813	JP 1992-14472	19920130
	JP 2753170	B2	19980518		
	US 5443030	A	19950822	US 1994-321470	19941011
PRAI	JP 1992-1449		19920108		
	JP 1992-14472		19920130		
	JP 1992-31853		19920219		
	JP 1992-31855		19920219		
	US 1992-998844		19921230		

AB A **cap** layer is formed on a Pb-containing ferroelec. film (e.g, PZT) formed on a substrate via a bottom capacitor electrode, and the Pb-containing ferroelec. film is crystallized by heating. The **cap** layer prevents vaporization of Pb from the ferroelec. film.

L16 ANSWER 19 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1992:534444 HCAPLUS
DN 117:134444
TI Sputter deposition of yttria-stabilized zirconia and silver cermet

electrodes for SOFC applications
AU Wang, L. S.; Thiele, E. S.; Barnett, S. A.
CS Dep. Mater. Sci., Northwestern Univ., Evanston, IL, 60208, USA
SO Solid State Ionics (1992), 52(1-3), 261-7
CODEN: SSIOD3; ISSN: 0167-2738
DT Journal
LA English
AB Y2O3-stabilized ZrO2 (YSZ) thin films were deposited by reactive magnetron sputter from a composite Zr-Y target in Ar-O mixts., for SOFC (solid-oxide fuel cell) use. YSZ deposition rates of 2.7 μm/h were obtained at a sputter source power of 150 W. Deposition with total pressure 3-20 mTorr yielded continuous, crack-free films in a compressive state of stress. X-ray diffraction and electron microscopy results showed that the films were polycryst. cubic YSZ with a columnar structure and an average grain diameter of 15 nm. Fully dense films with Ag electrodes showed that the O-ion conductivity was as expected for YSZ. Ag1-x[(Y2O3)0.1(ZrO2)0.9]x cermet thin films were deposited by reactive magnetron co-sputtering from Ag and Zr/Y targets in Ar-O mixts. The resistivity of as-deposited and **annealed** films as a function of Ag volume fraction fAg varied over several orders of magnitude. Evaporation of Ag from cermet films, observed during long-term **annealing** at 750°, was eliminated by depositing a 1 μm thick Sr-doped LaCoO3 **cap** layer on the cermet. The cermet with fAg ≈0.5 is a promising air electrode material for devices operating at ≤705°, exhibiting both low resistivity (1 + 10-4 Ω-cm) and high thermal stability.

L16 ANSWER 20 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1992:225604 HCAPLUS
DN 116:225604
TI Deposition, structure, and properties of cermet thin films composed of silver and yttrium-stabilized zirconia
AU Wang, L. S.; Barnett, S. A.
CS Dep. Mater. Sci. Eng., Northwestern Univ., Evanston, IL, 60208, USA
SO Journal of the Electrochemical Society (1992), 139(4), 1134-40
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
AB Ag1-x[(Y2O3)0.1(ZrO2)0.9]x (YSZ) cermet thin films were deposited by reactive magnetron cosputtering from Ag and Zr/Y targets in Ar-O2 mixts. The deposition conditions were such that the YSZ component in the films was fully oxidized. The film densities varied from ≈75% to >85% as the total pressure was decreased from 20 to 5 mTorr. Film resistivities ρ varied with Ag volume fraction fAg from 5 + 10-6 Ω-cm to >109 Ω-cm. For fAg < 0.4, ρ decreased rapidly with increasing fAg. For fAg > 0.4, ρ decreased more gradually with increasing fAg. The ρ in **annealed** films ranged from 4 + 10-4 Ω-cm for fAg = 0.4 to 5 + 10-6 Ω-cm for pure Ag. Long term (>100 h) **annealing** at ≥700° resulted in a gradual increase in cermet resistivity due to Ag evaporation and Ag segregation to surface islands. Both decomposition mechanisms were effectively suppressed at up to 750° by depositing a 1 μm thick porous perovskite **cap** layer on the cermet. Complex impedance spectroscopy measurements in air of cermet electrodes on YSZ electrolytes gave interfacial resistances that were a factor of ≈6 lower than those of pure Ag electrodes, e.g., 1.4 Ω-cm2 at 750°. Ag-YSZ

cermets thus have potential as high-conductivity, low-overpotential air electrode materials for solid-oxide electrochem. devices operating at temps. ≤750°.

L16 ANSWER 21 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1989:49778 HCAPLUS
DN 110:49778
TI Selective epitaxy of silicon having low interfacial level density with silica film
IN Kitajima, Hiroshi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 63198319	A2	19880817	JP 1987-29653	19870213
PRAI JP 1987-29653		19870213		

AB Si crystal film formation involves the following steps: (1) formation of an amorphous insulating film-bearing stabilized ZrO2 film on parts of a Si substrate; (2) selective growth of a Si film on bare parts of the substrate; (3) coating the Si film; and (4) **annealing** the substrate in an O-containing atmospheric after exposure of at least a part of the ZrO2 film surface. A stabilized ZrO2 film was formed on an oxide film-bearing Si substrate and coated with an oxide film, windows were formed in the ZrO2 film, a Si film was grown in the windows by selective epitaxy and coated with a SiO2 film, windows were formed in the oxide film on the ZrO2 film, and then the substrate was **annealed** in an O-containing atmospheric The ZrO2 film had high O-permeability and was useful for selective thermal oxidation of the interface of the side walls of the Si and SiO2 films by the **annealing** and gave decreased interfacial level d., and a n-MOS FET having a channel with low leakage current was prepared from the substrate.

L16 ANSWER 22 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1986:191691 HCAPLUS
DN 104:191691
TI Ceramic-metal engine parts
IN Matsui, Minoru; Tsuno, Nobuo
PA NGK Insulators, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 60180969	A2	19850914	JP 1984-35190	19840228
JP 05018779	B4	19930312		
PRAI JP 1984-35190		19840228		

AB A ceramic part is joined to an engine unit with the aid of a metal part. The metal part has an outer diameter smaller than that of the ceramic part

and a ring-shaped cut at the periphery on surface facing the ceramic part, and is fixed to the engine unit at the portion having the largest outer diameter Addnl., the metal part, which has a ring-shaped cut at the periphery and a smaller outer diameter than that of the ceramic part, is attached to the ceramic part such that the ring-shaped cut faces the ceramic part, and the metal part is fixed to the metal engine unit with the portion of the metal part which has the largest outer diameter and is finished. The ceramic part can be joined to the metal part by hot packing. The ceramic part can be joined to the metal part by a metalizing layer coated on the ceramic part or a metal buffer an the metalizing layer. The metal buffer on the metalizing layer may form a portion or all of the ring-shaped cut. The metal part attached to the ceramic part can be fixed to the metal engine unit by means of inlays or screws. At least one material for the ceramic part can be selected from ZrO2, Al2O3, Si3N4, SiC, or Sialon, and one material for the metal engine unit can be selected from cast iron, steel, and Al alloy. Thus, partially stabilized ZrO2 containing Y2O3 was fired and finished to a piston head. A Mo-Mn-SiO4-Al2O3 paste was applied to the surface of the protruding portion of the piston head and a metalizing layer was formed by **heat-treatment** in H2 containing water vapor, and the layer was Ni plated. A metal part was finished and joined to the ceramic part with a Ag solder.

L16 ANSWER 23 OF 23 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1986:154253 HCAPLUS
DN 104:154253
TI Phase equilibration in zirconia-yttria alloys by liquid-film migration
AU Chaim, R.; Heuer, A. H.; Brandon, D. G.
CS Dep. Metall. Mater. Sci., Case West. Reserve Univ., Cleveland, OH, 44106, USA
SO Journal of the American Ceramic Society (1986), 69(3), 243-8
CODEN: JACTAW; ISSN: 0002-7820
DT Journal
LA English
AB The tetragonal (t) and cubic (c) ZrO2 solid solns. in 2-phase ZrO2-8 weight% Y2O3 ceramics have low and high solute content, resp. **Annealing** 1600°-sintered samples at 700-1400° requires a change in the volume fraction of the coexisting phases, as well as their equilibrium Y2O3 content. The enrichment in Y2O3 content of the c-ZrO2 grains is accomplished by liquid-film migration involving the silicate grain-boundary phase, while the volume fraction of t-ZrO2 increases by the nucleation and growth of **cap**-shaped t-ZrO2 lenses. The interfaces between the c-ZrO2 matrix and the growing t-ZrO2 lenses are semicoherent.

L20 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:212143 HCAPLUS
DN 140:244914
TI **Barrier**-free copper interconnect fabrication
IN Lin, Jing-Cheng; Huang, Cheng-Lin; Shue, Winston; Liang, Mong-Song
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6706629	B1	20040316	US 2003-338120	20030107
PRAI	US 2003-338120		20030107		

AB The invention concs. on using copper as a metal interconnect medium, whereby the cost incurred by using copper can be reduced by eliminating the need for a conventional **barrier** layer, smooth sidewalls of the deposited copper can be obtained, reducing contact resistance, porous sidewalls between the created copper layer and surrounding low-k dielec. are sealed, and bonding between the created copper metal and the underlying interface is improved. A new method is provided is creating metal interconnect comprising Cu. A 1st embodiment of the invention provides for the application of a doped layer of Cu. A 2nd embodiment of the invention provides for the deposition of a Si nitride layer as an inter-**barrier** film over surfaces of an opening created in a layer of dielec. followed by removing the layer of Si nitride from the bottom of the opening followed by depositing a doped Cu-alloy seed layer over surfaces of the opening followed by plating a layer of Cu over the Cu-alloy seed layer.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L20 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:699285 HCAPLUS
DN 138:10252
TI Method for manufacturing a semiconductor memory device having a **zirconium oxide** layer as a hydrogen diffusion blocking layer
IN Lee, Seok Jae
PA Hynix Semiconductor Inc., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 2001004362	A	20010115	KR 1999-24992	19990628
PRAI	KR 1999-24992		19990628		

AB The method for manufacturing a semiconductor memory device having a **zirconium oxide** layer as a hydrogen diffusion blocking layer is provided to prevent hydrogen generated in a subsequent process from being diffused to an oxygen compound in a dielec. layer of a capacitor, by forming a ZrOx hydrogen diffusion blocking layer on the capacitor. A capacitor composed of a storage electrode, a dielec. layer and a plate

electrode is formed on a semiconductor substrate in which a transistor is formed. The dielec. layer can be made of a ferroelec. layer. A **zirconium oxide** layer as a hydrogen diffusion blocking layer is formed on the entire structure. A **thermal annealing process** is performed. A metal line is formed to connect the capacitor and the transistor. An interlayer dielec. is formed on the resultant structure. A **passivation** layer is formed on the interlayer dielec.

L20 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:694402 HCAPLUS
DN 132:8112
TI Effect of hydrogen **anneals** on niobium-doped lead zirconate titanate capacitors with **lanthanum** strontium cobalt **oxide**/platinum electrodes
AU Evans, Joe T., Jr.; Boyer, Leonard L.; Velasquez, Geri; Ramesh, Ramamoorthy; Aggarwal, Sanjeev; Keramidas, Vassillis
CS Radiant Technologies, Inc., Albuquerque, NM, 87106, USA
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1999), 38(9B), 5361-5363
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB Ferroelec. capacitors, being oxide ceramics, are very sensitive to the effects of hydrogen environments at elevated temps. [H. Ashida et al.: Integr. Ferroelectr. 21 (1998) 97]. After a capacitor has been exposed directly to a **annealing** hydrogen environment at low hydrogen partial pressures, the elec. properties of the device can deteriorate and leakage currents can increase. At higher hydrogen concentration gradients, such as the formidable forming gas **annealing**, phys. failure of the inter-layer dielec. (ILD) and/or top electrode adhesion can occur. The authors have examined various structural approaches to mitigate the effects of hydrogen damage on integrated ferroelec. lead zirconate titanate (PZT) capacitors. These approaches, including the use of a titanium dioxide **barrier** layer above the PZT to impede the reducing effect of hydrogen on the ceramic and the use of electrode layers other than platinum to eliminate the generation of free hydrogen ions by catalyst action [S. Aggarwal et al.: Appl. Phys. Lett. 73 (1998) 1973]. The authors have found that niobium-doped PZT capacitors using LSCO/platinum electrodes **passivated** with titanium dioxide will recover from 1% forming gas **annealing** within 30 min at 450°C in nitrogen.
RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2004:293080 HCAPLUS
DN 141:15298
TI Electron spin resonance characterization of defects at interfaces in stacks of ultrathin high-κ dielectric layers on silicon
AU Stesmans, A. L.; Afanas'ev, V. V.
CS Department of Physics and Astronomy, University of Leuven, Louvain, 3001, Belg.
SO Materials Research Society Symposium Proceedings (2004), 786(Fundamentals of Novel Oxide/Semiconductor Interfaces), 49-61
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB ESR anal. of (100)Si/SiOx/ZrO2, (100)Si/Al2O3 and Si/HfO2 structures with nm-thin dielec. layers deposited by different chemical vapor deposition procedures reveals, after hydrogen detachment, the presence of the trivalent Si dangling-bond-type centers Pb0, Pb1 as prominent defects in all entities. This Pb0, Pb1 fingerprint, generally unique for the thermal (100)Si/SiO2 interface, indicates that the as-deposited (100)Si/**metal oxides** interface is basically Si/SiO2-like.
Though sensitive to the deposition process, the Pb0 d. is found to be substantially larger than in standard (100)Si/SiO2. As probed by the Pb-type center properties, the Si/dielec. interfaces of all structures are under enhanced (unrelaxed) stress, typical for low temperature Si/SiO2 growth.
Standard
quality thermal Si/SiO2 properties in terms of Pb signature may be approached by appropriate **annealing** (≥650°C) in vacuum in the case of (100)Si/SiOx/ZrO2. Yet, O2 ambient appears required for Si/Al2O3 and Si/HfO2. It appears that Si/high-κ **metal oxide** structures with device grade quality interfaces can be realized with sub-nm thin SiOx interlayers. The d. of fast interface states closely matches the Pb0 d. variations, suggesting the center as the dominant fast interface trap. They may be efficiently **passivated** in H2 at 400°C.
RE.CNT 52 THERE ARE 52 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:777313 HCAPLUS
DN 139:269272
TI Process of **passivating** a **metal**-gated complementary **metal oxide** semiconductor
IN Callegari, Alessandro Cesare; D'Emic, Christopher P.; Kim, Hyungjun; McFeely, Fenton Read; Narayanan, Vijay; Yurkas, John Jacob
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003186518	A1	20031002	US 2002-99004	20020315
	US 6770500	B2	20040803		
PRAI	US 2002-99004		20020315		

AB The present invention is directed to a process of **passivating** a **metal**-gated complementary **metal oxide** semiconductor (CMOS) by lowering the interface state d. between the silicon substrate and the dielec. of the metal-gated CMOS structure and reducing the fixed charge in the dielec. More preferably, the present invention is directed to a process of **passivating** a metal-gated CMOS by exposing that CMOS to an atmospheric of mol. hydrogen at an elevated temperature higher than room temperature A process of **passivating** a metal-gated CMOS structure in which a metal-gated CMOS structure is **passivated** in an atmospheric of mol. H at a temperature of between .apprx.250° and .apprx.500° and a pressure of at least .apprx.200 torr. The present process provides a lower interface state d. than obtainable by prior art **passivation** processes.

L22 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:683633 HCAPLUS
DN 139:372612
TI Properties of ultrathin high-κ dielectrics on Si probed by electron spin resonance-active defects: Interfaces and interlayers
AU Stesmans, A.; Afanas'ev, V. V.
CS Department of Physics and Astronomy, University of Leuven, Louvain, 3001, Belg.
SO Proceedings - Electrochemical Society (2003), 2003-2(Silicon Nitride and Silicon Dioxide Thin Insulating Films), 66-78
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB An ESR anal. of (100)Si/SiOx/ZrO2, (100)Si/Al2O3 and Si/HfO2 structures with nm-thin dielec. layers grown by various chemical vapor deposition methods is presented. After photodesorption of **passivating** hydrogen the trivalent Si dangling-bond-type centers Pb0, Pb1 appear as prominent defects at all (100)Si/dielec. layers. While reassuring for the Si/SiOx/ZrO2 case, this Pb0, Pb1 fingerprint, generally unique for the thermal (100)Si/SiO2 interface, indicates that the as-deposited (100)Si/**metal oxides** interface is basically Si/SiO2-like. The nature of the interfaces/interlayers is particularly addressed. As probed by the properties of the Pb-type centers, the interfaces of all structures are found to be under enhanced (unrelaxed) stress, typical for low temperature Si/SiO2 growth. Standard quality thermal Si/SiO2 properties, as exposed by the Pb-type defects (d. .apprx.1+1012), may be approached by appropriate **annealing** (≥ 650°C) in vacuum in the case of (100)Si/SiOx/ZrO2. Yet, O2 ambient appears required for Si/Al2O3 and Si/HfO2. A minimal SiOx layer appears requisite. It appears that Si/high-κ **metal oxide** structures with device grade quality interfaces can be realized with sub-nm thin SiOx interlayers.
RE.CNT 39 THERE ARE 39 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 4 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:755186 HCAPLUS
DN 137:287660
TI Method of forming dielectric films on semiconductor wafers
IN Levy, Sagy; Bloom, Robin S.; Kepten, Avashai
PA Mattson Technology, Inc., USA
SO U.S. Pat. Appl. Publ., 23 pp.

CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002142624	A1	20021003	US 2001-957697	20010919
US 6638876	B2	20031028		
WO 2003030242	A1	20030410	WO 2001-US29831	20010919
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
EP 1340247	A1	20030903	EP 2001-975332	20010919
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR				
JP 2004523134	T2	20040729	JP 2003-533333	20010919
PRAI US 2000-233740P	P	20000919		
WO 2001-US29831	W	20010919		

AB A method for depositing a high-k dielec. coating onto a substrate, such as a semiconductor wafer, is provided. In 1 embodiment, the process is directed to forming a nitride layer on a substrate. In an alternative embodiment, the present invention is directed to forming a **metal oxide** or silicate on a semiconductor wafer. When forming a **metal oxide** or silicate, a **passivation** layer is 1st deposited onto the substrate.

L22 ANSWER 5 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:706030 HCAPLUS
DN 135:307044
TI Thermal analysis of nonisothermal **oxidation** parameters of **zirconium** powder
AU Sukharenko, Vladimir I.; Borisova, Lidia I.; Zhogova, Kira B.; Kremzukov, Ivan K.
CS Russian Federal Nuclear Centre, All-Russia Scientific Research Institute of Experimental Physics, Nizhniy Novgorod, 607190, Russia
SO High Temperatures - High Pressures (2001), 33(5), 557-561
CODEN: HTHPAK; ISSN: 0018-1544
PB Pion Ltd
DT Journal
LA English
AB The possibility of applying methods of DTA and TG to the study of nonisothermal **oxidn.** of **metals** was demonstrated, with Zr as an example. The Zr powders studied were produced by the Na thermal and electrolytic methods as well as by the electrolytic method with further grinding in a ball mill in alc. for different time intervals. **Zr oxidn.** covers several stages corresponding to the **oxidn.** of different-sized **Zr** particles, which is confirmed by the increase in the thermal effect for a fraction of small particles depending on time of grinding and by its decrease for a fraction of large ones. Grinding also affects heat evaluation rate and initial oxidation temperature, which is explained by the occurrence of a tribochem. effect.

To increase this effect, it is proposed to introduce a liquid **passivating** agent into the ground powders.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:585829 HCAPLUS
DN 135:171254
TI Electron spin resonance observation of Si dangling-bond-type defects at the interface of (100) Si with ultrathin layers of SiOx, Al2O3 and ZrO2
AU Stesmans, A.; Afanas'ev, V. V.
CS Department of Physics, University of Leuven, Louvain, 3001, Belg.
SO Journal of Physics: Condensed Matter (2001), 13(28), L673-L680
CODEN: JCOMEL; ISSN: 0953-8984
PB Institute of Physics Publishing
DT Journal
LA English
AB Paramagnetic point defects were probed by ESR in stacks of (100) Si with nm-thin SiOx, ZrO2, and Al2O3 layers. After photodesorption of **passivating** hydrogen (300 K; 8.48 eV), the Si dangling bond type interface centers Pb0, Pb1 appear as prominent defects at all (100) Si/dielec. interfaces, with Pb0 densities up to .apprx.6 + 1012 cm-2. This Pb0, Pb1 fingerprint, generally unique for the thermal (100) Si/SiO2 interface, indicates that, while reassuring for the Si/SiOx/ZrO2 case, the as-deposited (100)Si/Al2O3 interface is basically Si/SiO2-like. As probed by the Pb-type defects, the interfaces are under substantially enhanced stress, characteristic for low-temperature Si/SiO2 growth. Standard quality thermal Si/SiO2 interface properties, as exposed by the Pb-type defects (d. .apprx.1 + 1012 cm-2), may be approached by appropriate mild **annealing** (.apprx.650°). This fact of a naturally present or possibility to establish a high quality (100) Si/SiO2-type interface, with ultrathin SiO2 interlayer, may be basic to successful application of high-κ **metal oxides** in Si-based devices.

RE.CNT 31 THERE ARE 31 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:480647 HCAPLUS
DN 135:54543
TI Amorphous dielectric capacitors on silicon from dielectric films deposited directly on silicon and having low leakage and compatibility with CMOS fabrication
IN Duncombe, Peter Richard; Laibowitz, Robert Benjamin; Neumayer, Deborah Ann; Shaw, Thomas McCarroll
PA International Business Machines Corporation, USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6255122	B1	20010703	US 1999-300185	19990427
	US 2001014484	A1	20010816	US 2001-841947	20010425
	US 2001014505	A1	20010816	US 2001-841948	20010425
PRAI	US 1999-300185	A3	19990427		

AB High-capacity capacitors and gate insulators exhibiting moderately high dielec. consts. with surprisingly low leakage using amorphous or low temperature
films of perovskite type oxides including a titanate system material such as Ba titanate, Sr titanate, Ba Sr titanate (BST), lead titanate, lead zirconate titanate, lead La zirconate titanate, Ba La titanate, a niobate, aluminate or tantalate system material such as lead Mg niobate, Li niobate Li tantalate, K niobate and K Ta niobate, a W-bronze system material such as Ba Sr niobate, lead Ba niobate, Ba Ti niobate, and Bi-layered perovskite system material such as Sr Bi tantalate, Bi titanate deposited directly on a Si surface at temps. .apprx.450°. or less.
RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1997:244115 HCAPLUS
DN 126:230732
TI Long-lasting coated anodes for electrochemical processes, especially processes in acidic media, and their manufacture
IN Cardarelli, Francois; Comminellis, Christos; Leclerc, Olivier; Savall, Andre; Taxil, Pierre
PA Electricite De France, Fr.
SO Fr. Demande, 14 pp.
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2735386	A1	19961220	FR 1995-7158	19950615
	FR 2735386	B1	19970829		
PRAI	FR 1995-7158		19950615		

AB Of the anodes, consisting of a hollow metallic substrate provided with (a) an intermediate coating of an **oxide-passivated metal** and (b) an external coating of an electrocatalytic material, the substrate is selected from Cu, Ni, Ti, and stainless steel, the **oxide-passivated metal** is selected from Ta, Nb, Hf, Zr, and Ti, and the electrocatalytic material is selected from **metals** and/or their **oxides**. The anodes are manufactured by cleaning the substrate with surfactant and water, degreasing the cleaned substrate under reflux with hot chlorinated solvent, electrochem. polishing the substrate, rinsing the substrate with demineralized water, drying the substate with compressed air, electrochem. depositing an **oxide-passivated metal** in a bath of molten salts under inert atmospheric, removing the coated substrate from the bath, cooling the substrate under inert atmospheric, and cleaning the material, sandblasting and pickling the coated substrate to remove impurities and increase its sp. surface area, applying a solution containing the precursors of the next coating, evaporating the solvent by a drying stage, **heat-treating** the material at .apprx.450° for .apprx.5 min, repeating the coating operation 10 times, and **heat-treating** the material at .apprx.490° for 2 h. The anodes are especially suitable for use in the manufacture of Cl and NaOH (in this case the
electrocatalytic material preferably consists of RuO2 or a mixture or IrO2 and RuO2), in effluent treatment (in this case the electrocatalytic material preferably consists of PbO2 or SnO2), in organic electrosyntheses,

in preparative electrometallurgy, etc.

	TW 538528	B	20030621	TW 2002-91103955	20020304
	US 2003124794	A1	20030703	US 2002-318892	20021213
	JP 2003243526	A2	20030829	JP 2002-378532	20021226
PRAI	FR 2001-17069	A	20011231		

AB An electronic component comprising an integrated circuit is manufactured in a substrate and a planar capacitor, characterized in that the capacitor is manufactured on the level of **metalization** of the component, the **metalization** level forming a 1st electrode of the capacitor and that the capacitor comprises a 1st **barrier** diffusion layer for O, deposited above the top of the **metalization**, a stack of several different oxide layers, each layer presenting a thickness < 100 nm, the stack being deposited above the 1st **barrier** layer, a 2nd diffusion **barrier** layer for O deposited above the stack of **oxide** layers, and a **metallic** electrode above the 2nd **barrier** layer.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 8 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:491564 HCAPLUS
DN 139:55469
TI Metal current collect **protected** by oxide film for solid-state electrochemical devices
IN Jacobson, Craig P.; Visco, Steven J.; De Jonghe, Lutgard C.
PA The Regents of the University of California, USA
SO PCT Int. Appl., 23 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2003052858	A1	20030626	WO 2002-US40704	20021218
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
	US 2003170544	A1	20030911	US 2002-323136	20021218
	US 6740441	B2	20040525		
PRAI	US 2001-343330P	P	20011218		

AB Provided are low-cost, mech. strong, highly electronically conductive current collects and associated structures for solid-state electrochem. devices, techniques for forming these structures, and devices incorporating the structures. The invention provides solid state electrochem. devices having as current **interconnects** a ferritic steel felt or screen coated with a **protective** oxide film.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 9 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 2003:298767 HCAPLUS
DN 138:279837
TI Design and fabrication of a self-aligned ferroelectric memory transistor
IN Hsu, Sheng Teng; Li, Tingkai; Zhang, Fengyan
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 11 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1302978	A2	20030416	EP 2002-23155	20021015
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR, BG, CZ, EE, SK				
	US 2003071292	A1	20030417	US 2001-978487	20011016
	US 6673664	B2	20040106		
	JP 2003179214	A2	20030627	JP 2002-296738	20021009
	TW 571397	B	20040111	TW 2002-91123586	20021014
PRAI	US 2001-978487	A	20011016		

AB The invention relates to the design and fabrication of a self-aligned ferroelec. memory transistor. The fabrication process includes steps of (i) preparing a substrate, onto which are deposited a dielec. layer and a polysilicon layer, resp.; (ii) forming shallow trench isolation structures which extend through the polysilicon layer, the dielec. layer, and 500 nm of the substrate; (iii) depositing silicon oxide into the trenches; and (iv) forming a gate stack; (v) forming a sidewall **barrier** layer; (vi) depositing a layer of ferroelec. material; (vii) forming a top electrode structure on the ferroelec. material; and (viii) finishing the structure, including **passivation, oxide** deposition, and **metalization**.

L35 ANSWER 10 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:196916 HCAPLUS
DN 138:197185
TI Memory transistor and method of fabricating same
IN Hsu, Sheng Teng; Zhang, Fengyan; Li, Tingkai
PA Sharp Laboratories of America, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6531325	B1	20030311	US 2002-164785	20020604
	JP 2004015047	A2	20040115	JP 2003-54878	20030228
	US 2003222291	A1	20031204	US 2003-385038	20030310
	US 6703655	B2	20040309		
	EP 1369926	A2	20031210	EP 2003-253199	20030522
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR, BG, CZ, EE, HU, SK				
PRAI	US 2002-164785	A	20020604		

AB A ferroelec. memory transistor includes a substrate having active regions therein; a gate stack, including: a high-k insulator element, including a high-k cup and a high-k **cap**; a ferroelec. element, wherein said ferroelec. element is encapsulated within said high-k insulator element;

and a top electrode located on a top portion of said high-k insulator; a **passivation** oxide layer located over the substrate and gate stack; and **metalizations** to form contacts to the active regions and the gate stack. A method of forming a ferroelec. memory transistor includes preparing a substrate, including forming active regions and an oxide device isolation region; forming a gate placeholder structure in a gate region; removing the gate placeholder structure forming a gate void in the gate region; depositing a high-k insulator layer over the structure and in the gate void to from a high-k cup; filling the high-k cup with a ferroelec. material to form a ferroelec. element; depositing a high-k upper insulator layer and removing excess high-k material to form a high-k **cap** over the ferroelec. element; depositing a top electrode over the high-k **cap** to form a gate electrode and gate stack; depositing a layer of **passivation** oxide over the structure; etching the **passivation** oxide to from contact vias to the active regions and the gate stack; and metalizing the structure to complete the ferroelec. memory transistor.

RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 11 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:174117 HCAPLUS
DN 138:197159
TI In service programmable logic arrays with low tunnel **barrier** interpoly insulators
IN Forbes, Leonard
PA Micron Technology, Inc., USA
SO U.S. Pat. Appl. Publ., 37 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003042532	A1	20030306	US 2001-945512	20010830
	US 2004168145	A1	20040826	US 2004-788810	20040227
PRAI	US 2001-945512	A3	20010830		

AB Structures and methods for in service programmable logic arrays with low tunnel **barrier** interpoly insulators are provided which have improved flash memory densities and faster writing and erasing speeds. The in-service programmable logic array includes a 1st logic and a 2nd logic plan having a number of logic cells arranged in rows and columns that are **interconnected** to produce a number of logical outputs such that the in service programmable logic array implements a logical function. The logic cell includes a 1st source/drain region and a 2nd source/drain region separated by a channel region in a substrate. A floating gate opposing the channel region and is separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by a low tunnel **barrier** inter-gate insulator. The low tunnel **barrier** inter-gate insulator includes a **metal oxide** insulator selected from the group consisting of PbO, Al2O3, Ta2O5, TiO2, ZrO2, Nb2O5 and/or a Perovskite oxide tunnel **barrier** .

L35 ANSWER 12 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:770100 HCAPLUS
DN 137:287503

TI Process for making a MIM capacitor with recess in dielectric layer in semiconductor substrate
IN Roberts, Douglas R.; Luckowski, Eric
PA Motorola, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6461914	B1	20021008	US 2001-942208	20010829
WO 2003021661	A2	20030313	WO 2002-US25909	20020813
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
TW 558822	B	20031021	TW 2002-91119392	20020827
PRAI US 2001-942208	A	20010829		

AB A process for forming a metal-insulator-metal (MIM) capacitor structure includes forming a recess in the dielec. layer of a semiconductor substrate. A 1st capacitor electrode is formed in the recess having a copper 1st **metal** layer with a **conductive** oxidation **barrier** formed over the 1st metal layer. The 1st capacitor electrode is planarized relative to the dielec. layer. An insulator is formed over the 1st capacitor electrode and a 2nd capacitor electrode is formed over the insulator. Forming the 1st capacitor electrode in the recess maintains the alignment of a periphery of the copper 1st **metal** layer with the **conductive** oxidation **barrier**
.

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 13 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:669522 HCAPLUS
DN 137:209503
TI Plasma display panel with improved secondary electron emission characteristics
IN Katou, Akira; Kajiyama, Hiroshi; Uetani, Kazuo; Onisawa, Kenichi; Minemura, Tetsuro; Ihara, Yasushi; Takigawa, Shiro; Nose, Kouichi; Tokomoto, Isao; Koizumi, Yasuhiro
PA Hitachi, Ltd., Japan
SO Eur. Pat. Appl., 8 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1237175	A2	20020904	EP 2001-119738	20010827

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR

PRAI JP 2001-56996 A 20010301

AB The invention relates to a plasma display panel which has a front substrate having sustaining electrodes **wired** thereon and a rear substrate having address electrodes **wired** thereon and displays an image by means of elec. discharge that occurs in a minute discharge space formed in the gap between the 2 substrates and which has a **protective** film comprising at least one **metal oxide** which covers a dielec. layer provided to the front substrate, in which the **protective** film is constituted essentially of a material which undergoes elimination of the major part of moisture and CO2 adsorbed onto it at a temperature of 350° or less. The **protective** film comprises at least one oxide comprising Mg oxide as main component. Addnl. components may be selected from Ca, Sr, Ba, Zn, Al, Zr, Si, Ti, Sn, Ce and La. The plasma display panel has improved secondary electron emission characteristics.

L35 ANSWER 14 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:466646 HCAPLUS
DN 137:40266
TI Method of forming metal gate in semiconductor device
IN Lee, Sang Ick; Kim, Hyung Hwan; Jang, Se Aug
PA S. Korea
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002076867	A1	20020620	US 2001-994284	20011126
	JP 2002208698	A2	20020726	JP 2001-356533	20011121
PRAI	KR 2000-70219	A	20001124		

AB A method of forming a gate in a semiconductor device includes forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device, depositing a dummy gate polysilicon layer and a hard mask layer on the dummy gate insulating layer sequentially, patterning the hard mask layer into a mask pattern and patterning the dummy gate polysilicon layer using the mask pattern as an etch **barrier**, forming spacers at both sidewalls of the dummy gate polysilicon layer, depositing an insulating interlayer on the resultant structure after forming the spacers, exposing a surface of the dummy gate polysilicon layer by carrying out an oxide layer chemical-mech. polishing (CMP) process having a high selection ratio against the dummy gate polysilicon layer, forming a **damascene** structure by removing the dummy gate polysilicon layer and the dummy gate insulating layer using the insulating interlayer as another etch **barrier**, depositing a gate insulating layer and a gate metal layer on the entire surface of the semiconductor substrate having the **damascene** structure, and exposing a surface of the insulating interlayer by carrying out a metal CMP process having a high selection ratio against the insulating interlayer.

L35 ANSWER 15 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:291657 HCAPLUS
DN 136:312578

TI **Interconnector** for a high temperature fuel cell
IN Tietz, Frank; Gupta, Ashok; Teller, Oliver
PA Forschungszentrum Juelich G.m.b.H., Germany
SO Ger. Offen., 6 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 10050010	A1	20020418	DE 2000-10050010	20001010
PRAI	DE 2000-10050010		20001010		

AB A ceramic layer of manganese or cobalt oxide, or a mixed manganese oxide, is applied as thin **protective** layer on the steel **interconnector** of a fuel cell. It has the following advantageous characteristics: good elec. conductivity, slight porosity to prevent corrosion of the steel by air and eventual contamination of the cathode by Cr from the steel, and high chemical compatibility to avoid chemical reactions between **interconnector** steel and the contact layer that may form conductive corrosion products.

L35 ANSWER 16 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:158346 HCAPLUS
DN 136:209146
TI Methods of forming diffusion **barriers** for capacitor constructions in semiconductor circuits
IN Agarwal, Vishnu K.
PA USA
SO U.S. Pat. Appl. Publ., 12 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002025625	A1	20020228	US 1999-251104	19990216
	US 6387748	B2	20020514		
	US 6555863	B1	20030429	US 2000-566673	20000508
	US 2001039085	A1	20011108	US 2001-894320	20010627
	US 6638809	B2	20031028		
	US 2003189225	A1	20031009	US 2003-423423	20030425
	US 6780792	B2	20040824		
PRAI	US 1999-251104	A3	19990216		
	US 1999-251105	A1	19990216		
	US 2000-566673	A3	20000508		

AB The invention pertains to semiconductor circuit constructions, such as, for example capacitor constructions, and to methods of forming semiconductor circuit constructions. In particular aspects, the invention pertains to diffusion **barrier** layers for use in capacitor constructions. In 1 aspect, the invention encompasses a semiconductor circuit construction including a material which comprises Q, R, S and B. In such construction, Q comprises ≥1 refractory metals, R is selected from the group consisting of ≥1 of W, Al and Si, S is selected from the group consisting of ≥1 of N and O, and B is B. Also, in such construction R and Q do not comprise a common element. In another aspect, the invention encompasses a method of forming a capacitor.

A 1st capacitor electrode is formed, a diffusion **barrier** layer is formed proximate the 1st capacitor electrode, and a dielec. layer is formed to be separated from the 1st capacitor electrode by the diffusion **barrier** layer. A 2nd capacitor electrode is formed to be separated from the 1st electrode by the dielec. layer. The diffusion **barrier** layer comprises QxRySz in which Q is a refractory metal, R is selected from the group consisting of W, Al and Si, and S is selected from the group consisting of N and O; provided that R is not the same element as Q. The formation of the diffusion **barrier** layer comprises depositing the QxRySz and exposing the QxRySz to a N-containing plasma.

L35 ANSWER 17 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:123570 HCAPLUS
DN 136:176548
TI Slurry for chemical mechanical polishing of metal layer, method of preparing the slurry, and **metallization** method using the slurry
IN Lee, Jong-Won; Yoon, Bo-Un; Hah, Sang-Rok
PA S. Korea
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002019128	A1	20020214	US 2001-816365	20010326
PRAI	KR 2000-30800	A	20000605		

AB A slurry for use in chemical mech. polishing (CMP) of a metal layer. The CMP slurry includes an abrasive, a plurality of oxidizing agents, a stabilizer including an organic acid having a carboxyl group, a corrosion inhibitor which suppresses corrosion of a metal, a F compound which reduces a difference in removal rates of a metal layer and a **barrier** layer, and deionized H2O. The plurality of oxidizing agents include a 2nd oxidizing agent which **oxidizes** the **metal** and a 1st **oxidizing** agent which restores an oxidizing ability of the 2nd oxidizing agent.

L35 ANSWER 18 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:630922 HCAPLUS
DN 135:188771
TI Double layer electrode and **barrier** system on hemispherical grain silicon for use with high dielectric constant materials and methods for fabricating the same
IN Al-Shareef, Husam N.; Deboer, Scott; Thakur, Randhir
PA Micron Technology, Inc., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6281543	B1	20010828	US 1999-386833	19990831
	US 2001039097	A1	20011108	US 2001-892594	20010627
	US 6399459	B2	20020604		
	US 2002155658	A1	20021024	US 2002-159892	20020530

US 6673689 B2 20040106
PRAI US 1999-386833 A3 19990831
US 2001-892594 A1 20010627
AB A high surface area capacitor comprising a double metal layer (an electrode metal and **barrier** material) deposited on hemispherical grain (HSG) Si, in which a high dielec. constant (HDC) material is deposited over the double metal layer. The high surface area capacitor is complete with an upper cell plate electrode deposited over the HDC material. The double metal layer is preferably comprises 1 noble metal, such as Pt or Pd, for the electrode **metal** and an **oxidizable metal**, such as Ru, Ir, or Mo, for the **barrier** material. The noble metal, such as Pt metal, alone would normally allow O diffusion into and oxidize any adhesion layer (making the adhesion layer less conductive) and/or undesirably oxidize any Si-containing material during the deposition of the HDC material. Thus, the **barrier** metal is used to form a conducting oxide layer or a conducting layer which stops the O diffusion. The HSG Si provides an enhanced surface roughness that boosts cell capacitance. The HDC material, preferably BST or the like, is also used to boost cell capacitance.
RE.CNT 30 THERE ARE 30 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 19 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:401353 HCAPLUS
DN 135:130575
TI Hydrogen-robust submicron IrOx/Pb(Zr,Ti)O3/Ir capacitors for embedded ferroelectric memory
AU Sakoda, Tomoyuki; Moise, Theodore S.; Summerfelt, Scott R.; Colombo, Luigi; Xing, Guoqiang; Gilbert, Stephen R.; Loke, Alvin L. S.; Ma, Shawming; Kavari, Rahim; Wills, Laura A.; Amano, Jun
CS Si Technology Development, Texas Instruments Inc., Dallas, TX, 75243, USA
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2001), 40(4B), 2911-2916
CODEN: JAPNDE; ISSN: 0021-4922
PB Japan Society of Applied Physics
DT Journal
LA English
AB The authors demonstrated that the scaling of IrOx(Pb(Zr,Ti)O3:PZT)/Ir capacitors can be extended into the submicron regime. The submicron IrOx/PZT/Ir capacitors were fabricated using a 1-mask stack-etch process, integrated with an SiO2 interlayer dielec., and contacted with Al **metalization**. The aggregate elec. properties of integrated PZT capacitor arrays are nearly independent of individual capacitor area in the range between 102μm2 and 0.12μm2. In particular, switched polarization values of >30 μC/cm2 were obtained for PZT capacitors with an individual capacitor area of 0.12μm2. This result suggests that the lateral scaling can be achieved down to 0.1μm2. Through the use of appropriate diffusion **barriers**, H-robust submicron PZT capacitors are obtained. No degradation in ferroelec. properties of submicron PZT capacitors was observed under the test conditions. These results suggest that PZT capacitors can be integrated into a standard complementary **metal oxide** semiconductor (CMOS) process flow with minimal degradation
RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 20 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 2000:786189 HCAPLUS
DN 134:60185
TI Preparation of **protective oxidation** layer of **metallic interconnector** for solid **oxide** fuel cells
AU Kim, Sang-Woo; Lee, Byong-Ho; Lee, Jong-Ho
CS Creamic Processing Research Center, KIST, Seoul, 136-791, S. Korea
SO Han'guk Seramik Hakhoechi (2000), 37(9), 887-893
CODEN: HSHAF7
PB Korean Ceramic Society
DT Journal
LA Korean
AB Oxidation properties of antioxidn. layer-coated ferritic steel were investigated for application as metallic **interconnectors** of an intermediate temperature range solid oxide fuel cell (SOFC). Ferritic steel showed that elec. resistance was highly increased with time owing to its surface chromium oxide and iron oxide layer formed by high temperature oxidation
However, **lanthanum** manganese **oxide** (LMO) coated Ferritic steel showed the increase with a periodical increase and decrease of high temperature resistance such as Ducrolloy, and did not show further the increase of resistance with time by forming a anti-oxidation layer after 80 h. It was explained that LMO coated Ferritic steel had long-term stability for high temperature oxidation

L35 ANSWER 21 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:117214 HCAPLUS
DN 132:169766
TI Metalizing of heat-resistant powders or substrates by mechanical coating with a metal compound followed by hot reduction
IN Fokina, Elena Leonidovna; Budim, Nadezhda Ivanovna; Chernik, Galina Georgievna
PA Russia
SO PCT Int. Appl., 13 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000008220	A1	20000217	WO 1999-RU254	19990714
	W: AE, AL, AU, BA, BG, BR, CA, CN, CZ, EE, HR, HU, ID, IL, IN, JP, KR, LT, LV, MK, PL, RO, SG, SI, SK, US, VN, YU, ZA, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	RU 2149217	C1	20000520	RU 1998-113972	19980717
	AU 2000015884	A1	20000228	AU 2000-15884	19990714
PRAI	RU 1998-113972	A	19980717		
	WO 1999-RU254	W	19990714		

AB Adherent metal coating is applied on the surface of degreased dry powders or substrates by: (a) mech. coating with oxide, hydroxide, or sulfide of Cu, Ni, Al, Zn, Ti, W, Ge, Au, Co, Mo, Sn, Pd, and/or Pt; and (b) reduction of the compound layer to metal by heating in a non-oxidizing atmospheric to nominally 200-500°. The heat-resistant powders or substrates are optionally coated by milling in the presence of the precursor slurry, especially at

200-300°. The process is based on solid-phase reactions, and is suitable for metalizing of abrasives, ceramics, or semiconductors. Synthetic diamond powder (size .apprx.50 μm) was mixed with Cu oxide at the diamond:Cu weight ratio of 1:1 by milling for 20 min, and the oxide-coated powder was heated at 450° in Ar for the oxide dissociation, cooled, and treated by CF2C12 for stability, resulting in the adherent Cu coating ≥3 μm thick on the diamond powder.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 22 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:69477 HCAPLUS
DN 130:189930
TI Effects of CeO2 incorporation on the performance of a Ta diffusion **barrier** for Al **metalization**
AU Kim, Jaehwa; Kwak, Joon Seop; Yoon, Dong-Soo; Baik, Hong Koo; Lee, Sung-Man
CS Department of Metallurgical Engineering, Yonsei University, Seoul, 120-749, S. Korea
SO Journal of Applied Physics (1999), 85(4), 2170-2174
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB The effects of CeO2 incorporation on the performance of a Ta diffusion **barrier** in the Al/Si system were investigated in the temperature range of 450-550°. When the Ta film was deposited without CeO2 incorporation, the reaction between Ta and Al occurred at 500°, leading to the formation of Al3Ta. In the case of CeO2-incorporated Ta **barriers**, however, the reaction between Ta and Al was suppressed up to 550°. The suppression of the reaction of Ta with Al is attributed to the strong chemical bonding of Ta-Ce-O or Ta-O and the amorphous-like microstructure of the CeO2-incorporated Ta **barrier**, followed by the reduction of the chemical driving force for the initial stage of Al3Ta formation.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 23 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:326243 HCAPLUS
DN 129:61288
TI Stabilized platinum electrodes for ferroelectric film deposition using Ti, Ta, and Zr adhesion layers
AU Maeder, T.; Sagalowicz, L.; Muralt, P.
CS Laboratoire Ceramique, Ecole Polytechnique Federale Lausanne, Lausanne, CH-1015, Switz.
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1998), 37(4A), 2007-2012
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB Pt-based **metalizations** using different adhesion layers (Ti, Zr, and Ta) were studied for use as electrodes for ferroelec. thin films on oxidized silicon substrates. Different ways of oxidizing the adhesion layers prior to ferroelec. film growth are compared, with regard to obtaining stable, adherent Pt films of well-defined (111) orientation,

while avoiding leading diffusion through the electrode. Upon in-situ deposition of PbTiO3 at high excess lead flux, lead diffusion through the Pt films was found to depend strongly on the adhesion layer and the stabilization treatment. Pre-oxidation reduces lead diffusion during the later processing. Ti diffuses through the electrode upon **oxidn** ., whereas Ta and **Zr** stay in place, in analogy to the diffusivities in the corresponding oxides. A novel oxidation treatment was developed to produce stable, adherent **metalizations** with controlled orientation and good **barrier** properties against lead diffusion.

RE.CNT 23 THERE ARE 23 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 24 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1996:691608 HCAPLUS
DN 125:334017
TI Volatility of chromium from **interconnect** material
AU Weiss, R.; Peck, D.; Miller, M.; Hilpert, K.
CS Research Centre Julich, Institute Materials Energy Systems, Juelich, 52425, Germany
SO High Temperature Electrochemistry: Ceramics and Metals, Proceedings of the Risoe International Symposium on Materials Science, 17th, Roskilde, Den., Sept. 2-6, 1996 (1996), 479-484. Editor(s): Poulsen, F. W. Publisher: Risoe National Laboratory, Roskilde, Den.
CODEN: 63PAA2
DT Conference
LA English
AB Acceptor doped LaCrO3 and alloys are generally considered as materials for the ceramic and **metallic interconnect** in solid **oxide** fuel cells (SOFC). MgO, CaO and SrO are used as dopants in LaCrO3. The alloys used as metallic **interconnect** contain Cr in order to render possible the formation of a chromia scale for corrosion **protection**. The Ni or Fe based alloys considered contain 15-30 mass percent Cr. Novel Cr based alloys are, addnl., of interest; for example the oxide dispersion strengthened (ODS) alloy Cr5Fe1Y2O3. It has been shown by various groups that the use of chromium containing alloys for the **interconnect** can lead to a rapid degradation of the elec. properties of a SOFC due to chromium vaporization. Chromium vaporization may also lead to a degradation of the elec. properties if a ceramic **interconnect** is used since they are also made of chromium containing materials. The possible sealant constituents sodium and potassium can lead to a substantial increase of the Cr vaporization by the formation of Na2CrO4 and K2CrO4.

L35 ANSWER 25 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:424999 HCAPLUS
DN 121:24999
TI Aluminum nitride circuit board and method of producing it
IN Horiuchi, Michio; Hayashi, Koichiro; Harayama, Yoichi
PA Shinko Electric Industries Co. Ltd., Japan
SO Eur. Pat. Appl., 18 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	EP 587382	A2	19940316	EP 1993-306988	19930903
	EP 587382	A3	19941123		
	EP 587382	B1	19980311		
	R: DE, FR, GB				
	JP 06085461	A2	19940325	JP 1992-262928	19920905
	JP 3171695	B2	20010528		
	JP 06097630	A2	19940408	JP 1992-266735	19920909
	JP 06125153	A2	19940506	JP 1992-299192	19921012
	KR 125101	B1	19971204	KR 1993-14823	19930731
	CA 2105448	AA	19940306	CA 1993-2105448	19930902
	US 5464950	A	19951107	US 1993-115767	19930903
PRAI	JP 1992-262928	A	19920905		
	JP 1992-266735	A	19920909		
	JP 1992-299192	A	19921012		

AB The board includes an AlN ceramic body. An inner **conductor metal** which is to be used as a **wiring** material is formed in the aluminum nitride ceramic body. The inner **conductor metal** is mainly made of Cu, the m.p. of which is lower than the firing temperature of the AlN ceramic. A layer mainly made of a Group IVB metal or compound, such as Ti, Zr, or Hf, may be formed as an interface between the AlN ceramic body and the inner **conductor metal** to improve wetting of the AlN and thereby contact and adhesion between them. Alternatively the Group IVB metal or compound may be mixed with the **conductor metal** precursor. Further **protective** green sheets of AlN used to prevent vaporization of the **conductor metal** during firing may be replaced by a thin AlN paste layer which still **protects** the **conductor metal** but which is easier to remove subsequently. Finally the tracks in the ceramic body which are filled with the **conductor metal** may include a pot to provide a reservoir to accommodate addnl. **conductor metal** material to compensate for any shrinkage of it or loss which occurs on firing.

L35 ANSWER 26 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1993:178201 HCAPLUS
DN 118:178201
TI Breakaway oxidation in materials for nuclear reactors
AU Kirillov, I. A.; Fridman, A. A.; Rusanov, V. D.
CS Kurchatov Inst. At. Energy, Moscow, 123182, Russia
SO Proc. Eur. Conf. Adv. Mater. Processes, 2nd (1992), Meeting Date 1991, Volume 3, 163-9. Editor(s): Clyne, T. W.; Withers, P. J. Publisher: Inst. Mater., London, UK.
CODEN: 58TYAG
DT Conference
LA English
AB The renewed interest in the breakaway oxidation process is motivated by need for refinement of the physicochem. models of coolant-cladding interaction under severe accident conditions. In order to obtain a quant. theor. description of the long-term **oxidn.** kinetics of steam-**zirconium** reaction and fuel cladding behavior the concept of autowave is introduced. Steady post-breakaway movement of the **oxide/metal** interface is interpreted as normal reaction frontpropagation, autocatalyzed by scale degradation due to permanent formation of an **interconnected** macrodefect system. Using both the Barenblatt condition for defect equilibrium in a nonuniform oxide stress field and percolation criterion for oxide scale degradation, the anal.

dependence of the breakaway oxidation rate coefficient, **barrier** layer thickness and characteristic crack length upon temperature and mechano-chemical oxide parameters were obtained. Comparison of theor. calcns. with existing exptl. data have shown a good agreement. The proposed theor. framework and models could lead to new developments in the description of the breakaway oxidation in materials for nuclear reactors and which may be used in safety anal. and computer simulations.

L35 ANSWER 27 OF 27 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1992:138202 HCAPLUS
DN 116:138202
TI Oxide characteristics and their relationship to hydrogen uptake in zirconium alloys
AU Warr, Brian D.; Elmoselhi, M. B.; Newcomb, S. B.; McIntyre, N. S.; Brennenstuhl, A. M.; Lichtenberger, P. C.
CS Res. Div., Ontario Hydro, Toronto, ON, W8Z 5S4, Can.
SO ASTM Special Technical Publication (1991), 1132(Zirconium Nucl. Ind.), 740-57
CODEN: ASTTA8; ISSN: 0066-0558
DT Journal
LA English
AB SIMS and TEM have been used to investigate composition and structure of **oxides** on pure **zirconium** and Zr-2.5Nb following both in and out-reactor exposures in aqueous and gaseous environments. Thin oxides formed in steam at 400° on Zr-2.5Nb act as excellent hydrogen permeation **barriers** for CANDU pressure tubes. Following up to 4350 effective full power days (EFPD) exposure in-reactor in the annulus gas, and out-reactor elevated exposures to deuterium gas, these oxides generally continue to show diffusional-type through-thickness deuterium concentration profiles, with negligible deuterium contents at the **metal /oxide** interface. Diffusion coeffs. inferred from these profiles are as low as .apprx.2 + 10-22 m2/s at 300°. The structure of these thin **oxides** on **Zr**-2.5Nb consists of columnar grains with amorphous regions at grain boundaries and at the **metal/oxide** interface, and non-**interconnected** porosity, which implies that deuterium permeation is likely controlled by solid state diffusion through the bulk oxide. At regions containing relatively high deuterium contents in the bulk metal of removed pressure tubes, outside surface oxides showed several regions with flat deuterium concentration profiles with higher deuterium concns. at the **metal/ oxide** interface. Examination of thicker oxides with **interconnected** porosity, on pure Zr, following exposures to pure deuterium gas, also showed the presence of flat deuterium concentration profiles.

This would tend to suggest that regions of high deuterium concentration dissolved in the base metal of pressure tubes may also contain oxides with **interconnected** porosity.

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SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC 1969-2004/Aug W5
         (c) 2004 Institution of Electrical Engineers
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  File   8:Ei Compendex(R) 1970-2004/Aug W5
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  File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
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         (c) 2004 ProQuest Info&Learning
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  File  94:JICST-EPlus 1985-2004/Aug W2
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  File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jul
         (c) 2004 The HW Wilson Co.
  File 144:Pascal 1973-2004/Aug W5
         (c) 2004 INIST/CNRS
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         (c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs 1970-2004/Aug
         (c) 2004 DECHEMA
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200457
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2004/May(Updated 040903)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
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Set	Items	Description
S1	38844	(CE OR CERIUM)(3N)OXID? OR CEO
S2	31381	(LA OR LANTHANUM)(3N)OXID? OR LAO
S3	48400	(ZR OR ZIRCONIUM)(3N)OXID?
S4	9739	(S1 OR S2 OR S3) AND (ANNEAL? OR RTP OR RTA OR (HEAT? OR THERMAL?)(3N)(PROCESS? OR TREAT?))
S5	2723	S4 AND METAL?(3N)(OXID? OR CONDUCT?)
S6	172	S5 AND (CAP OR CAPING OR PASSIVAT? OR BARRIER? OR PROTECT?)
S7	7	S6 AND (INTER()CONNECT? OR INTERCONNECT? OR METALIZAT? OR METALLIZAT? OR METALLISAT? OR METALISAT? OR WIRING OR WIRED OR DAMASCEN? OR DUAL()DAMASCEN? OR DUALDAMASCEN?)
S8	7	RD (unique items)
S9	165	S6 NOT S7
S10	9	S9 AND (CAP OR CAPING)
S11	9	RD (unique items)
S12	156	S9 NOT S10
S13	0	S12 AND (METALIZAT? OR METALLIZAT? OR METALLISAT? OR METALISAT?)
S14	0	S12 AND (WIRING OR WIRED)
S15	0	S12 AND (DAMASCEN? OR DUAL()DAMASCEN?)
S16	56	S12 AND ANNEAL?
S17	53	RD (unique items)
S18	13	S17 AND S1
S19	40	S17 NOT S18
S20	15	S19 AND S2
S21	8	S20 AND S3
S22	7	S20 NOT S21
S23	7	RD (unique items)
S24	25	S19 NOT S20
S25	25	S24 AND S3
S26	0	S25 AND (INTER()CONNECT? OR INTERCONNECT?)
S27	25	S25
S28	25	RD (unique items)
S29	571401	METAL?(3N)(OXID? OR CONDUCT?)
S30	20594	S29 AND (S1 OR S2 OR S3)

8/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03469819 JICST ACCESSION NUMBER: 98A0177156 FILE SEGMENT: JICST-E
The Hysteresis Caused by Interface Trap and Anomalous Positive Charge in Al/CeO2-SiO2/Silicon Capacitors.
ROH Y (1); KIM K (1); JUNG D (1)
(1) Sung Kyun Kwan Univ., Suwon, KOR
Jpn J Appl Phys Part 2, 1997, VOL.36,NO.12B, PAGE.L1681-L1684, FIG.3, REF.11
JOURNAL NUMBER: F0599BAD ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3 548.4:621.315.592 539.211:621.315.592
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: We report the hysteresis induced by two similar defects located at and near the SiO2-Si interface in the Al/CeO2-SiO2/Si capacitor. We find that the hysteresis are generated directly due to the presence of interface trap and anomalous positive charge. Electrical characteristics of the hysteresis are, however, distinct and are strongly dependent on the type of defects. For example, the hysteresis caused by interface traps disappeared after **passivating** the Si dangling bonds by a post **metallization annealing**, while only a bias-temperature **annealing** causes the reduction of the hysteresis generated by anomalous positive charge. We suggest the mechanisms of the hysteresis generation in the Al/CeO2-SiO2/Si capacitor. (author abst.)

8/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016272490
WPI Acc No: 2004-430384/200440
XRAM Acc No: C04-161089
XRPX Acc No: N04-340277
Formation of hafnium and/or zirconium film on substrate, involves vaporizing hafnium and/or **zirconium alkoxide** precursor into vaporized precursor, and depositing constituent of vaporized precursor on substrate at preset temperature
Patent Assignee: CABRAL C (CABR-I); CALLEGARI A C (CALL-I); GRIBELYUK M A (GRIB-I); JAMISON P C (JAMI-I); LACEY D L (LACE-I); MCFEELY F R (MCFE-I); NARAYANAN V (NARA-I); NEUMAYER D A (NEUM-I); RANADE P (RANA-I); ZAFAR S (ZAFA-I)
Inventor: CABRAL C; CALLEGARI A C; GRIBELYUK M A; JAMISON P C; LACEY D L; MCFEELY F R; NARAYANAN V; NEUMAYER D A; RANADE P; ZAFAR S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040092073	A1	20040513	US 2002291334	A	20021108	200440	B

Priority Applications (No Type Date): US 2002291334 A 20021108

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20040092073 A1 28 H01L-021/4763

Abstract (Basic): US 20040092073 A1
Abstract (Basic):

NOVELTY - A precursor mixture comprising hafnium and/or **zirconium alkoxide** precursor and a liquid is used in the method of forming film on substrate. At least hafnium and/or **zirconium alkoxide** precursor is vaporized into a vaporized precursor. A constituent of the vaporized precursor is deposited on surface of substrate at deposition temperature of greater than 400degreesC to form a film.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) microcrystalline film comprising hafnium **oxide** and/or ***zirconium*** ***oxide*** . The film comprises little or no Fourier transform infrared (FTIR) detectable carbon or hydroxyl group, and has grain size of 10 nm or less; and

(2) an electronic device including at least the film located on surface of the substrate.

USE - For formation of hafnium and/or zirconium film on substrate for electronic device such as transistors, capacitors, diodes, resistors, switches, light emitting diodes, lasers, **wiring** structures, ***interconnect*** structures.

ADVANTAGE - The film is dense, smooth, microcrystalline and is capable of self-**passivation** when treated in a hydrogen plasma ***passivation*** or forming gas ***anneal*** . The film is stable under reducing condition and forms device of excellent electrical properties with minimal flat band voltage shift, appropriate threshold voltage, low inversion thickness and enhanced mobility. The number of interface states with minimal or no loss of accumulation capacitance is reduced by utilizing hydrogen plasma **passivation** or forming gas ***anneal*** . Reduction of hydroxyl group and carbon in the film and suppression of interfacial oxides corresponds to improved electrical properties, less interfacial states, fewer traps, lower leakage and improved dielectric constant.

DESCRIPTION OF DRAWING(S) - The figure shows the illustration of cross-sectional view of integrator circuit of p-type field effect transistor and n-type field effect transistor.

substrate (10)
p-type conductive region (13)
gate electrode (14,19)
gate dielectric (15)
n-type conductive region (18)
pp; 28 DwgNo 1/29

8/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015724806
WPI Acc No: 2003-787006/200374
Related WPI Acc No: 2003-576925; 2003-688634; 2004-303447; 2004-410352; 2004-439895; 2004-569548
XRAM Acc No: C03-217016

XRPX Acc No: N03-630664
Integrated circuit includes hydrogen **barrier** layer comprising strontium tantalate, bismuth tantalate, tantalum **oxide**, titanium **oxide**, **zirconium oxide**, or aluminum **oxide**

Patent Assignee: SYMETRIX CORP (SYME-N)
Inventor: CELINSKA J; JOSHI V; MCMILLAN L D; PAZ DE ARAUJO C A; SOLAYAPPAN N

Number of Countries: 102 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030098497	A1	20030529	US 2001998469	A	20011129	200374	B
WO 200349147	A2	20030612	WO 2002US37694	A	20021122	200374	
AU 2002357755	A1	20030617	AU 2002357755	A	20021122	200419	
US 6781184	B2	20040824	US 2001998469	A	20011129	200457	

Priority Applications (No Type Date): US 2001998469 A 20011129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030098497	A1		23	H01L-023/58	
WO 200349147	A2	E		H01L-000/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

AU 2002357755	A1		H01L-023/58	Based on patent WO 200349147
US 6781184	B2		H01L-027/108	

Abstract (Basic): US 20030098497 A1
Abstract (Basic):

NOVELTY - An integrated circuit comprises a thin film of **metal oxide** material, and a hydrogen **barrier** layer (80) located to inhibit the diffusion of hydrogen to the **metal** ***oxide*** material. The hydrogen ***barrier*** layer comprises strontium tantalate, bismuth tantalate, tantalum **oxide**, titanium ***oxide*** , ***zirconium*** ***oxide*** , or aluminum ***oxide***

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of making an integrated circuit device comprising depositing a **metal oxide** film on a substrate, forming a hydrogen **barrier** layer on the thin film, and performing an integrated circuit fabrication process using hydrogen.

USE - Used as an integrated circuit.

ADVANTAGE - The hydrogen **barrier** layer does not increase gain growth when subjected to high temperature recovery **anneals**, thus decreasing manufacturing defects caused by expanding layer within an integrated circuit. It can be deposited on top of first metal layer without compromising the **metallization** and retains its electrical and hydrogen **barrier** properties throughout conventional integrated circuit processing steps.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional diagram of an integrated circuit with a hydrogen ***barrier*** layer.

Substrate (50)
Metal oxide (70)
Electrodes (76)

Capacitor (78)
Hydrogen **barrier** layer (80)
pp; 23 DwgNo 2/14

8/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015668629
WPI Acc No: 2003-730816/200369
XRAM Acc No: C03-201004
XRPX Acc No: N03-584164
Capacitor production for dynamic random access memory, comprises forming including capacitor dielectric film of **metal oxide**, depositing interlayer insulating film, and forming opening in region of insulating film
Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: ITO T
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030143804	A1	20030731	US 2002321475	A	20021218	200369	B
JP 2003224245	A	20030808	JP 200223406	A	20020131	200369	
CN 1435877	A	20030813	CN 2003101674	A	20030114	200373	
US 6730560	B2	20040504	US 2002321475	A	20021218	200430	

Priority Applications (No Type Date): JP 200223406 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030143804	A1		27	H01L-021/8242	
JP 2003224245	A		18	H01L-027/105	
CN 1435877	A			H01L-021/82	
US 6730560	B2			H01L-021/8242	

Abstract (Basic): US 20030143804 A1
Abstract (Basic):

NOVELTY - The production of a semiconductor comprises forming on a substrate (101) a capacitor device including a capacitor dielectric film of **metal oxide**, depositing an inter-layer insulating film of an oxide on the capacitor device, and forming opening in the region of the insulating film above the capacitor device and forming on the insulating film a conducting film connected to the capacitor device.

DETAILED DESCRIPTION - The production of a semiconductor device on a substrate involves forming a capacitor device including a capacitor dielectric film of **metal oxide**, depositing an inter-layer insulating film of an oxide on the capacitor device, and forming an opening in a region of the insulating film above the capacitor device and forming on the insulating film a conducting film connected to the capacitor device through the opening in such manner that a portion of the insulating film above a periphery of the capacitor device is exposed. During a convey time, the substrate is being conveyed or during a wait time before or after the conveying of the substrate, the substrate on which the conducting film is formed is contained in a container an atmosphere within which has a lower moisture concentration

than ambient atmosphere until a whole top face of the insulating film is covered with another member.

USE - Used in the production of a semiconductor device.

ADVANTAGE - The process prevents electric characteristic of capacitor dielectric film including ferroelectric of **metal oxide** from being degraded by moisture desorbed from insulating film through ***annealing*** .

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional view of the production of a semiconductor device.

First container (10)
Semiconductor substrate (101)
Interconnect (111B)
Protection film (112)
Contact hole (113a)
Second **interconnect** (114B)
pp; 27 DwgNo 6B/12

8/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014595854
WPI Acc No: 2002-416558/200244
XRAM Acc No: C02-117507
XRPX Acc No: N02-327789

Fabrication of **metal oxide** semiconductor field effect transistor device involves utilizing dummy gate region during implantation, activation **annealing** and siliciding of source and drain regions

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC); IBM UK LTD (IBMC)
Inventor: BOYD D C; BRODSKY S B; HANAFI H I; ROY R A
Number of Countries: 099 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200227799	A2	20020404	WO 2001GB4154	A	20010917	200244	B
JP 2002151690	A	20020524	JP 2001286248	A	20010920	200250	
AU 200187877	A	20020408	AU 200187877	A	20010917	200252	
US 6440808	B1	20020827	US 2000672185	A	20000928	200259	
EP 1320878	A2	20030625	EP 2001967502	A	20010917	200341	
			WO 2001GB4154	A	20010917		
KR 2003033081	A	20030426	KR 2003704228	A	20030324	200354	
TW 517288	A	20030111	TW 2001123593	A	20010925	200356	

Priority Applications (No Type Date): US 2000672185 A 20000928
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200227799	A2	E	19	H01L-029/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

JP 2002151690	A		9	H01L-029/78	
AU 200187877	A			H01L-029/00	Based on patent WO 200227799

US 6440808 B1 H01L-021/336
EP 1320878 A2 E H01L-021/336 Based on patent WO 200227799
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
KR 2003033081 A H01L-021/334
TW 517288 A H01L-021/28

Abstract (Basic): WO 200227799 A2
Abstract (Basic):

NOVELTY - A sub-0.1 microns ***metal*** ***oxide*** semiconductor field effect transistor device is fabricated via **damascene**-gate processing technique which includes the use of a dummy gate region that is present during implanting, activation **annealing** and siliciding the source and drain regions.

DETAILED DESCRIPTION - Fabrication of a sub-0.1 microns ***metal*** **oxide** semiconductor field effect transistor device involves:

(a) providing a dummy gate region on a surface of a semiconductor substrate (10) that includes a polysilicon sandwiched between its bottom and top oxide layers;

(b) forming activated source and drain regions on the substrate using the dummy gate region as an implantation mask;

(c) siliciding the surface of the substrate overlying the activated source and drain regions;

(d) forming an insulator layer on the substrate's surface to surround the dummy gate;

(e) planarizing the insulator layer to remove the top oxide layer, thus exposing the polysilicon;

(f) selectively removing the polysilicon and the bottom oxide layer to provide an opening which exposes a portion of the substrate;

(g) forming a gate dielectric on the exposed substrate's portion;

(h) depositing a gate conductor on the gate dielectric layer; and

(i) etching the insulator layer.

USE - For fabricating sub-0.1 microns MOSFET.

ADVANTAGE - Enables decoupling of the gate implantation and activation **annealing** from the source and drain implantation and activation ***annealing*** . The resulting high-performance sub-0.1 microns MOSFET devices have a minimum polysilicon-, i.e., poly-, depletion, silicided source and drain junctions and very low sheet resistance (on the order of at least 5 ohm/sq.) polygates and that is independent of the silicidation process of the source and drain regions.

DESCRIPTION OF DRAWING(S) - The drawing shows a pictorial representation of a high-performance sub-0.1 microns MOSFET device.

substrate (10)
source and drain extensions (36)
spacers (38)
source and drain regions (40)
gate dielectric (48)
optional liner (50)
conductive material (52)
pp; 19 DwgNo 12/14

8/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014292629
WPI Acc No: 2002-113331/200215
Related WPI Acc No: 2002-279333
XRAM Acc No: C02-034750
XRPX Acc No: N02-084419

Fabrication of ferroelectric capacitor device for memory devices by using non-ferroelectric insulating layer or conducting layer, or by forming capacitor with specific aspect ratio or without patterning ferroelectric material

Patent Assignee: ADVANCED TECHNOLOGY MATERIALS (ADTE-N)
Inventor: BILODEAU S M; BUSKIRK P C V; VAN BUSKIRK P C

Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010035543	A1	20011101	US 99264047	A	19990308	200215	B
			US 2001893155	A	20010627		
US 6511856	B2	20030128	US 99264047	A	19990308	200311	
			US 2001893155	A	20010627		

Priority Applications (No Type Date): US 99264047 A 19990308; US 2001893155 A 20010627
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010035543	A1		12	H01L-029/76	Cont of application US 99264047
US 6511856	B2			H01L-021/00	Cont of application US 99264047

Abstract (Basic): US 20010035543 A1
Abstract (Basic):

NOVELTY - A ferroelectric capacitor device is fabricated with the ferroelectric material capacitor element confining E-fields by either depositing a non-ferroelectric, high epsilon material insulating layer; depositing a conducting layer on stack capacitor; forming stack capacitor without patterning the ferroelectric material; or forming the ferroelectric stack capacitor with specific aspect ratio.

DETAILED DESCRIPTION - Fabrication of a ferroelectric capacitor device involves forming a ferroelectric stack capacitor (8) with ferroelectric material capacitor element on a substrate containing buried transistor circuitry. The transistor circuitry is beneath an insulation layer having via containing a conductive plug to the transistor circuitry.

E-fields are confined to the ferroelectric capacitor material element by:

(a) patterning the stack capacitor, and depositing a non-ferroelectric, high epsilon material insulating layer (12) over and on the sides of the stack capacitor;

(b) patterning the stack capacitor, depositing an insulating capping layer on the patterned stack capacitor to prevent electrical short-circuiting between top and bottom electrodes of the capacitor, and depositing a conducting layer over and on the sides of the stack capacitor;

(c) forming the stack capacitor without patterning the ferroelectric material so that the deposited ferroelectric material comprises a region aligned with top and bottom electrodes defining ferroelectric capacitor material element and ferroelectric material outside the region, and rendering the ferroelectric material outside of the region non-ferroelectric; or

(d) forming the ferroelectric stack capacitor with an aspect ratio,

of effective lateral dimension of the ferroelectric capacitor material element to a thickness of the ferroelectric capacitor material element, that is greater than 5.

USE - For forming ferroelectric capacitor device (claimed) for (ferroelectric) dynamic random access memories useful for 0.18mum and smaller feature size applications.

ADVANTAGE - Unwanted dispersion of E-fields into regions surrounding the ferroelectric material is avoided. The method enables formation of high density memory arrays from conventional ferroelectric materials without deleterious cross-talk and other interference phenomena that result from dispersion of E-fields beyond capacitor loci.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of a stack capacitor array.

Ferroelectric stack capacitor (8)

Non-ferroelectric, high epsilon material insulating layer (12)

pp; 12 DwgNo 1/2

8/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012275668
WPI Acc No: 1999-081774/199908
XRAM Acc No: C99-074836
XRPX Acc No: N99-190131

Rapid heating element has a palladium-doped gold resinate resistive line

Patent Assignee: SCHAFFLER & CO GMBH (SCHA-N)
Inventor: OCHSENHOFER K; SMETANA W
Number of Countries: 083 Number of Patents: 013
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
AT 9701677	A	19990115	AT 971677	A	19971003	199908	B
WO 9918586	A1	19990415	WO 98AT233	A	19981002	199922	
AT 405591	B	19990715	AT 971677	A	19971003	199933	
AU 9894236	A	19990427	AU 9894236	A	19981002	199936	
EP 1023735	A1	20000802	EP 98947223	A	19981002	200038	
			WO 98AT233	A	19981002		
BR 9814811	A	20001003	BR 9814811	A	19981002	200053	
			WO 98AT233	A	19981002		
KR 2001030871	A	20010416	KR 2000703562	A	20000401	200163	
US 6316752	B1	20011113	WO 98AT233	A	19981002	200173	
			US 2000509964	A	20000510		
JP 2001519595	W	20011023	WO 98AT233	A	19981002	200202	
			JP 2000515281	A	19981002		
MX 2000003269	A1	20010601	MX 20003269	A	20000403	200235	
EP 1023735	B1	20020807	EP 98947223	A	19981002	200259	
			WO 98AT233	A	19981002		
DE 59805128	G	20020912	DE 505128	A	19981002	200264	
			EP 98947223	A	19981002		
			WO 98AT233	A	19981002		
ES 2179534	T3	20030116	EP 98947223	A	19981002	200316	

Priority Applications (No Type Date): AT 971677 A 19971003
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

AT 9701677 A H05B-003/12
WO 9918586 A1 G 18 H01C-017/065
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
AT 405591 B H05B-003/12 Previous Publ. patent AT 9701677
AU 9894236 A H01C-017/065 Based on patent WO 9918586
EP 1023735 A1 G H01C-017/065 Based on patent WO 9918586
Designated States (Regional): DE ES FR GB IT
BR 9814811 A H01C-017/065 Based on patent WO 9918586
KR 2001030871 A H01C-017/065
US 6316752 B1 H05B-003/16 Based on patent WO 9918586
JP 2001519595 W 16 H01C-017/06 Based on patent WO 9918586
MX 2000003269 A1 H01C-001/142
EP 1023735 B1 G H01C-017/065 Based on patent WO 9918586
Designated States (Regional): DE ES FR GB IT
DE 59805128 G H01C-017/065 Based on patent EP 1023735
Based on patent WO 9918586
ES 2179534 T3 H01C-017/065 Based on patent EP 1023735

Abstract (Basic): WO 9918586 A1
Abstract (Basic):

NOVELTY - A rapid heating element (100) has an AuPd or Au resinate resistive line (103) with overlapping contact areas (104, 104') of a thick film AgPd or PdAu ***metallization*** .

DETAILED DESCRIPTION - A rapid heating element (100) comprises a substrate (101) bearing a structured AuPd or Au resinate resistive layer (103), overlapping end contact areas (104, 104') of a thick film AgPd or PdAu **conductive metallization** and stud-like solder-stop **barriers** (105, 105') on the contact areas (104, 104').

An INDEPENDENT CLAIM is also included for producing a rapid heating element (100), used for igniting propellant charges, by (a) screen printing, drying and sintering a glass or glass-ceramic paste on an alumina ceramic substrate; (b) repeating step (a) until the desired thickness is achieved and preferably lapping and polishing to acceptable surface roughness; (c) **heat treating** the substrate to avoid micro-crack formation; (d) screen printing, drying and firing an AuPd or Au resistive resinate paste; (e) structuring the resistive layer by wet chemical etching or sputter etching; (f) screen printing, drying and sintering a conductive paste which overlaps the resistive line; (g) **heat treating** the substrate for controlled resistance alteration and stabilization; and (h) screen printing, drying and sintering a glass paste as a stud structure on the conductive contacts.

USE - As a rapid heating element useful for igniting propellant charges of airbag systems.

ADVANTAGE - The Pd doping allows the sheet resistance of the AuPd resinate resistive layer, having a predetermined thickness of 0.1-1.5 microns, to be varied in the range 300 mohms to 3 ohms without the need for changing the layer thickness.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a preferred heating element.

Heating element (100)

Substrate (101)
Glass-ceramic coating (102)
Resistive line (103)
Thick film **conductive metallization** (104, 104')
Solder-stop **barriers** (105, 105')
pp; 18 DwgNo 1/1

18/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7843069 INSPEC Abstract Number: A2004-05-7780D-004, B2004-03-2810D-001
Title: Improved Characteristics of ultrathin **CeO**/sub 2/ by using postnitridation **annealing**
Author(s): Jer Chyi Wang; Yen Ping Hung; Chung Len Lee; Tan Fu Lei
Author Affiliation: Dept. of Electron. Eng., Nat. Chiao-Tung Univ., Hsinchu, Taiwan
Journal: Journal of the Electrochemical Society vol.151, no.2 p. F17-21
Publisher: Electrochem. Soc,
Publication Date: Feb. 2004 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(200402)151:2L.f17:ICUC;1-M
Material Identity Number: J010-2004-001
U.S. Copyright Clearance Center Code: 0013-4651/2004/151(2)/F17/5/$7.00
Language: English
Abstract: This work demonstrates the improved characteristics of an ultrathin **CeO**/sub 2/ dielectric by using the post-N/sub 2/O plasma **treatment** with additional rapid **thermal** N/sub 2/ ***annealing*** . The ***CeO*** /sub 2/ after the treatment exhibits superior characteristics such as a small effective oxide thickness (~2.25 nm), a low leakage current (5.4*10/sup -4/ A/cm/sup 2/), a high breakdown electric field (-24 MV/cm), a long projected 10 yr lifetime (-12 MV/cm), a small capacitance-voltage hysteresis (25 mV), and a high **barrier** height for Frenkel-Poole emission (0.55 eV). These good properties are attributed to the nitrogen incorporation into the dielectric to eliminate the traps after ***annealing*** . The postnitridation ***annealing*** appears to be a very useful treatment for future ultrathin **metal-oxide** gate dielectrics.
Subfile: A B

18/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7483986 INSPEC Abstract Number: A2003-03-8160B-067
Title: Enhanced corrosion resistance of magnesium and its alloys through the formation of **cerium** (and aluminium) **oxide** surface films
Author(s): Ardelean, H.; Fiaud, C.; Marcus, P.
Author Affiliation: Lab. de Physico-Chimie des Surfaces, Ecole Nat. Superieure de Chimie, Paris, France
Journal: Materials and Corrosion vol.52, no.12 p.889-95
Publisher: Wiley-VCH Verlag GmbH,
Publication Date: 2001 Country of Publication: Germany
CODEN: MTCREQ ISSN: 0947-5117
SICI: 0947-5117(2001)52:12L.889:ECRM;1-P
Material Identity Number: D323-2002-012
U.S. Copyright Clearance Center Code: 0947-5117/01/1212-0889$17.50+.50/0
Language: English
Abstract: **Cerium** (and aluminium) **oxide** layers were formed on magnesium and its alloys (AZ91) by chemical surface treatment with or

without subsequent ***annealing*** . The corrosion behaviour modifications provided by the formation of these surface films were studied by means of different electrochemical and surface analysis techniques. The electrochemical behaviour, studied in sodium sulphate (Na/sub 2/SO/sub 4/) solution, showed (i) a marked shift of the corrosion potential towards more positive values, (ii) a slight inhibition of the cathodic reaction and (iii) a significant decrease of the anodic dissolution current. X-ray photoelectron spectroscopy (XPS) was used for the characterisation of the composition of the deposited films and of the changes in the film composition during the electrochemical corrosion tests. The components of some **oxide** films are **cerium** dioxide (**CeO** /sub 2/), aluminium oxide (Al/sub 2/O/sub 3/) and aluminium hydroxide (AI(OH)/sub 3/). Other ***metallic*** mixed ***oxide*** films were obtained as a function of the solution composition. Very little (or no) change in the oxide film composition during the cathodic and anodic polarization experiments was observed from XPS measurements. Chemical treatment provides thick and moderately adherent ***protective*** oxide films. ***Annealing*** under oxygen further improves the beneficial effect of the chemical treatment.
Subfile: A

18/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06746559
E.I. No: EIP04108049337
Title: Improved Characteristics of Ultrathin **CeO** //2 by Using Postnitridation **Annealing**
Author: Wang, Jer Chyi; Hung, Yen Ping; Lee, Chung Len; Lei, Tan Fu
Corporate Source: Dept. of Electronics Engineering National Chiao-Tung University, Hsinchu 300, Taiwan
Source: Journal of the Electrochemical Society v 151 n 2 2004. p F17-F21
Publication Year: 2004
CODEN: JESOAN ISSN: 0013-4651
Language: English
Abstract: This work demonstrates the improved characteristics of an ultrathin **CeO**//2 dielectric by using the post-N//2O plasma ***treatment*** with additional rapid ***thermal*** N//2 ***annealing*** . The **CeO**//2 after the treatment exhibits superior characteristics such as a small effective oxide thickness (similar to 2.25 nm), a low leakage current (5.4 multiplied by 10 **-**4 A/cm**2), a high breakdown electric field (-24 MV/cm), a long projected 10 yr lifetime (-12 MV/cm), a small capacitance-voltage hysteresis (25 mV), and a high **barrier** height for Frenkel-Poole emission (0.55 eV). These good properties are attributed to the nitrogen incorporation into the dielectric to eliminate the traps after ***annealing*** . The postnitridation ***annealing*** appears to be a very useful treatment for future ultrathin **metal**-***oxide*** gate dielectrics. copy 2004 The Electrochemical Society. All rights reserved. 22 Refs.

18/3,AB/4 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

16514247 PASCAL No.: 04-0160460
Improved characteristics of ultrathin **CeO** SUB 2 by using postnitridation **annealing**
JER CHYI WANG; YEN PING HUNG; CHUNG LEN LEE; TAN FU LEI
Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan
Journal: Journal of the Electrochemical Society, 2004, 151 (2) F17-F21
Language: English
This work demonstrates the improved characteristics of an ultrathin **CeO** SUB 2 dielectric by using the post-N SUB 2 O plasma **treatment** with additional rapid **thermal** N SUB 2 **annealing** . The ***CeO*** SUB 2 after the treatment exhibits superior characteristics such as a small effective oxide thickness (similar 2.25 nm), a low leakage current (5.4 x 10 SUP - SUP 4 A/cm SUP 2), a high breakdown electric field (-24 Mv/cm), a long projected 10 yr lifetime (-12 MV/cm), a small capacitance-voltage hysteresis (25 mV), and a high **barrier** height for Frenkel-Poole emission (0.55 eV). These good properties are attributed to the nitrogen incorporation into the dielectric to eliminate the traps after ***annealing*** . The postnitridation ***annealing*** appears to be a very useful treatment for future ultrathin **metal-oxide** gate dielectrics.

18/3,AB/5 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

09588609 PASCAL No.: 91-0379052
Phase stability of zirconia-based thermal ***barrier*** coatings. II, Zirconia-ceria alloys
BRANDON J R; TAYLOR R
UMIST, Manchester materials sci. cent., Manchester Greater Manchester M1 7HS, United Kingdom
Journal: Surface & coatings technology, 1991, 46 (1) 91-101
Language: English
Des revetements de zircone alliee avec 12, 15, 20 et 25% de **CeO** SUB 2 ont ete prepares par projection plasma et recuits a des temperatures comprises entre 1200 et 1600 Degree C. Les structures des phases ont ete analysees et comparees avec celles d'echantillons non vieillis.

18/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016205773
WPI Acc No: 2004-363659/200434
Related WPI Acc No: 2003-329299; 2003-502736
XRAM Acc No: C04-137192
XRPX Acc No: N04-290838
Manufacture of integrated circuits for use in capacitor structures and memory devices, comprises oxidizing region(s) of second metal layer to form **metal oxide** regions corresponding to grain boundaries of first metal layer

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: BASCERI C; SANDHU G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040058491	A1	20040325	US 2000711206	A	20001109	200434	B
			US 2002227662	A	20020826		
			US 2003669384	A	20030924		

Priority Applications (No Type Date): US 2000711206 A 20001109; US 2002227662 A 20020826; US 2003669384 A 20030924
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040058491	A1		17	H01L-021/8242	Div ex application US 2000711206 Cont of application US 2002227662 Div ex patent US 6534357

Abstract (Basic): US 20040058491 A1
Abstract (Basic):

NOVELTY - Manufacture of integrated circuits comprises:

(i) forming a first metal layer on at least a portion of oxygen-containing surface portion of a substrate assembly;

(ii) forming a second metal layer on the first metal layer;

(iii) providing an oxidation diffusion **barrier** layer;

(iv) oxidizing region(s) of the second metal layer to form **metal oxide** regions corresponding to grain boundaries of first metal layer; and

(v) removing the oxidation diffusion ***barrier*** layer.

DETAILED DESCRIPTION - Manufacture of integrated circuits comprises:

(a) forming a first metal layer (24) on at least a portion of oxygen-containing surface portion of a substrate assembly;

(b) forming a second metal layer on the first metal layer;

(c) providing an oxidation diffusion **barrier** layer on a portion of the second metal layer;

(d) oxidizing region(s) of the second metal layer to form **metal oxide** regions corresponding to grain boundaries (26) of first metal layer by **thermally treating** the substrate assembly having the two **metal** layers, and **oxidation** diffusion **barrier** layer; and

(e) removing the oxidation diffusion **barrier** layer and unoxidized portions of the second metal layer.

USE - For manufacture of integrated circuits, for use in capacitor structures and memory devices (e.g. dynamic random access memory).

ADVANTAGE - The method uses the diffusion of oxygen through the grain boundaries of the platinum layer to obtain a composite bottom electrode that includes platinum layer and local ruthenium oxide regions formed on grain boundaries. The composite platinum/ruthenium oxide electrode is a **barrier** to oxygen diffusion during high temperature process in oxidizing atmospheres. Oxygen diffusion through the grain boundaries of the platinum layer is prevented by having the ruthenium regions of the grain boundaries of the platinum material. The composite electrode also acts as a sink for oxygen vacancies in high permittivity oxide materials. This provides for improved dielectric performance, e.g. improved resistance degradation lifetime or fatigue for ferroelectric oxide dielectrics.

DESCRIPTION OF DRAWING(S) - The figure shows the capacitor

structure using the **metal/metal oxide** composite electrode.
First metal layer (24)
Grain boundaries (26, 63)
Dielectric material (62)
Second electrode (64)
pp; 17 DwgNo 3/4

18/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015973056
WPI Acc No: 2004-130897/200413
Related WPI Acc No: 2002-557192
XRAM Acc No: C04-052236
XRPX Acc No: N04-104375
Formation of integrated circuit capacitor by encapsulating upper capacitor electrode and capacitor dielectric with **protective** layer, then patterning the **protective** layer and electrode layer to define lower capacitor electrode
Patent Assignee: LEE K (LEEK-I)
Inventor: LEE K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030211687	A1	20031113	US 2001900269	A	20010706	200413 B
			US 2003455132	A	20030605	

Priority Applications (No Type Date): KR 200079189 A 20001220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030211687	A1		9	H01L-021/8242	Div ex application US 2001900269 Div ex patent US 6603169

Abstract (Basic): US 20030211687 A1
Abstract (Basic):
NOVELTY - An integrated circuit capacitor is formed by:
(a) patterning an electrode layer as an upper capacitor electrode and a capacitor dielectric layer as a capacitor dielectric;
(b) encapsulating the upper capacitor electrode and the capacitor dielectric with a **protective** layer; and
(c) patterning the **protective** layer and the first electrode layer to define a lower capacitor electrode and expose an upper surface of the interlayer dielectric layer.
DETAILED DESCRIPTION - Formation of integrated circuit capacitor involves:
(a) forming an interlayer dielectric layer (110) on a semiconductor substrate (100);
(b) sequentially forming a first electrode layer on the interlayer dielectric layer, a capacitor dielectric layer comprising a ferroelectric material on an upper surface of the first electrode layer (130') and a second electrode layer on the capacitor dielectric layer;
(c) patterning the second electrode layer as an upper capacitor electrode and the capacitor dielectric layer as a capacitor dielectric and exposing the upper surface of the first electrode layer;

(d) encapsulating the upper capacitor electrode and the capacitor dielectric by depositing a **protective** layer (160') on the upper surface of the first electrode layer and on the upper capacitor electrode and the capacitor dielectric, the **protective** layer comprising a material that is free of hydrogen and has a chemical and/or physical structure that blocks transfer of hydrogen; and

(e) patterning the **protective** layer and the first electrode layer to define a lower capacitor electrode and expose an upper surface of the interlayer dielectric layer.

USE - Forming an integrated circuit capacitor.

ADVANTAGE - The process preserves the hysteresis characteristics of the ferroelectric materials.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of intermediate structure.

Substrate (100)
Interlayer dielectric layer (110)
Electrode layer (130')
Ferroelectric layer pattern (140)
Protective layer (160')
pp; 9 DwgNo 6/7

18/3,AB/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015440594
WPI Acc No: 2003-502736/200347
Related WPI Acc No: 2003-329299; 2004-363659
XRAM Acc No: C03-134239
XRPX Acc No: N03-398995

Fabrication of integrated circuits, e.g. capacitor structures, involves oxidizing region(s) of second metal layer, to form **metal oxide** regions corresponding to one or more grain boundaries of first metal layer

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: BASCERI C; SANDHU G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6534357	B1	20030318	US 2000711206	A	20001109	200347	B

Priority Applications (No Type Date): US 2000711206 A 20001109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6534357	B1		13	H01L-021/8242	

Abstract (Basic): US 6534357 B1
Abstract (Basic):

NOVELTY - Fabrication of integrated circuits involves forming first metal layer on at least a portion of oxygen-containing surface portion of substrate assembly; forming a second metal layer on a portion of the first **metal** layer; and **oxidizing** region(s) of the second metal layer, to form **metal oxide** regions corresponding to one or more grain boundaries of the first metal layer.

DETAILED DESCRIPTION - Fabrication of integrated circuits involves forming a first metal layer (13) on at least a portion of oxygen-containing surface (18) portion of substrate assembly (17);

forming a second metal layer (15) on a portion of the first **metal** layer; providing an **oxidation** diffusion **barrier** layer on at least a portion of the second **metal** layer; **oxidizing** region(s) of the second metal layer to form **metal oxide** regions (16) corresponding to one or more grain boundaries (14) of the first metal layer by **thermally treating** the substrate assembly having the first metal layer, second **metal** layer, and **oxidation** diffusion **barrier** layer (20); and removing the oxidation diffusion **barrier** layer and unoxidized portions of the second metal layer.

USE - For use in fabrication of integrated circuits, e.g. capacitor structures and memory devices (dynamic random access memory devices).

ADVANTAGE - During high temperature oxidization processes, such as those used to form a high dielectric constant material, oxygen diffusion through the grain boundaries of the platinum layer is prevented by having the ruthenium oxide regions on the grain boundaries of the platinum material. The composite platinum/ruthenium oxide electrode also acts as a sink for oxygen vacancies in high permittivity oxide materials. This provides for improved dielectric performance, e.g. improved resistance degradation lifetime or fatigue, for ferroelectric oxide dielectrics.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional schematic of a substrate assembly having a composite **metal/** ***metal*** ***oxide*** ***conductive*** structure, as above.

First metal layer (13)
Grain boundaries (14)
Second metal layer (15)
Metal oxide regions (16)
Substrate assembly (17)
Surface (18)
Oxygen diffusion **barrier** layer (20)
pp; 13 DwgNo 1/4

18/3,AB/9 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014885102
WPI Acc No: 2002-705808/200276
Related WPI Acc No: 2002-470184
XRAM Acc No: C02-200173
XRPX Acc No: N02-556395

Non-aqueous metal organic liquid precursor solution for forming transparent ***metal*** ***oxide*** thin film layers, e.g. fluorescent lamps or flat panel displays, comprises organic precursor compound containing metal

Patent Assignee: SYMETRIX CORP (SYME-N)
Inventor: BACON J W; CELINSKA J; CUCHIARO J D; MCMILLAN L D; PAZ DE ARAUJO C A
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020087018	A1	20020704	US 99388044	A	19990901	200276	B
			US 200137877	A	20011109		
US 6686489	B2	20040203	US 99388044	A	19990901	200414	
			US 200137877	A	20011109		

Priority Applications (No Type Date): US 99388044 A 19990901; US 200137877 A 20011109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020087018	A1		21	C07F-005/00	Div ex application US 99388044 Div ex patent US 6376691
US 6686489	B2			C07F-019/00	Div ex application US 99388044 Div ex patent US 6376691

Abstract (Basic): US 20020087018 A1
Abstract (Basic):

NOVELTY - Providing novel precursors for forming transparent **metal oxide** thin film layers in a fluorescent lamp, flat panel display or other electrooptical device.

DETAILED DESCRIPTION - A non-aqueous metal organic liquid precursor solution comprises an organic precursor compound containing a first metal which can be tin, antimony, indium, cerium, yttrium, titanium, zirconium, hafnium, silicon, niobium, tantalum, or bismuth.

INDEPENDENT CLAIMS are included for the following:

(a) a method of preparing the above liquid precursor solution, comprising mixing a **metal alkoxide** and a carboxylic acid in an organic solvent to form a reaction mixture containing a first metal, and reacting the reaction mixture to form a metal carboxylate containing the first metal; and

(b) a method of making a **metal oxide**, comprising applying the above liquid precursor to a substrate to form a film on the substrate, and treating the film to form a solid film of the ***metal*** ***oxide*** .

USE - For forming transparent **metal oxide** thin film layers (44, 46) in electrooptical devices, e.g. fluorescent lamps (10) or flat panel displays.

ADVANTAGE - The inventive liquid precursor solution forms transparent **metal oxide** thin films that inhibit the generation of measles or black spot defects, in fluorescent lamps, thus improving their appearance and operating performance. It also provides greater efficiency and control in the manufacture of the thin films in electrooptical devices.

DESCRIPTION OF DRAWING(S) - This shows a cross-sectional diagrammatic view of a lamp wall of a fluorescent lamp.

Fluorescent lamp (10)

Metal oxide thin film layers (44, 46)

pp; 21 DwgNo 2/15

18/3,AB/10 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014736488
WPI Acc No: 2002-557192/200259
Related WPI Acc No: 2004-130897
XRAM Acc No: C02-157967
XRPX Acc No: N02-441098

Integrated circuit capacitor for memory devices comprises **protective** layer encapsulating upper capacitor electrode and capacitor dielectric layer and blocking transfer of hydrogen

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); LEE K (LEEK-I)
Inventor: LEE G M; LEE K
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020074588	A1	20020620	US 2001900269	A	20010706	200259 B
JP 2002203949	A	20020719	JP 2001300294	A	20010928	200262
KR 2002049875	A	20020626	KR 200079189	A	20001220	200282
US 6603169	B2	20030805	US 2001900269	A	20010706	200353

Priority Applications (No Type Date): KR 200079189 A 20001220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020074588	A1		10	H01L-027/108	
JP 2002203949	A		7	H01L-027/105	
KR 2002049875	A			H01L-027/105	
US 6603169	B2			H01L-029/72	

Abstract (Basic): US 20020074588 A1
Abstract (Basic):

NOVELTY - An integrated circuit capacitor comprises a **protective** layer that encapsulates the upper capacitor electrode and the capacitor dielectric layer. The ***protective*** layer comprises a hydrogen-free material having a chemical and/or physical structure that blocks transfer of hydrogen.

DETAILED DESCRIPTION - An integrated circuit capacitor comprises a semiconductor substrate; a lower capacitor electrode on the substrate; a capacitor dielectric layer comprising a ferroelectric material on the lower capacitor electrode; an upper capacitor electrode on the capacitor dielectric layer; and a **protective** layer that encapsulates the upper capacitor electrode and the capacitor dielectric layer. The ***protective*** layer comprises a hydrogen-free material having a chemical and/or physical structure that blocks transfer of hydrogen. An INDEPENDENT CLAIM is included for a method of forming an integrated circuit capacitor by forming an interlayer dielectric layer (110) on a semiconductor substrate (100); sequentially forming a first electrode layer (130'), a capacitor dielectric layer (140) and a second electrode layer (150); patterning the second electrode layer as an upper capacitor electrode and the capacitor dielectric layer as a capacitor dielectric and exposing the upper surface of the first electrode layer; encapsulating the upper capacitor electrode and the capacitor dielectric by depositing a **protective** layer (160') on the upper surface of the first electrode layer and on the upper capacitor electrode and the capacitor dielectric; and then patterning the **protective** layer and the first electrode layer to define a lower capacitor electrode and expose an upper surface of the interlayer dielectric layer.

USE - For memory devices.

ADVANTAGE - By blocking the infiltration of hydrogen, the hysteresis characteristics of the ferroelectric materials can be preserved.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an intermediate structure in the manufacture of a ferroelectric capacitor of a semiconductor memory device.

Semiconductor substrate (100)
Interlayer dielectric layer (110)
First electrode layer (130')

Capacitor dielectric layer (140)
Second electrode layer (150)
Protective layer (160')
pp; 10 DwgNo 6/7

18/3,AB/11 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014470658
WPI Acc No: 2002-291361/200233
XRAM Acc No: C02-085441
XRPX Acc No: N02-227496
Integrated circuit memory device, e.g., ferroelectric random access memory device, has dielectric regions **protected** with multilayer insulation structures
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); AN H (ANHH-I); CHO H (CHOH-I)
Inventor: AHN H G; CHO H J; AN H; CHO H
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020021544	A1	20020221	US 2001923670	A	20010807	200233	B
JP 2002100742	A	20020405	JP 2001235332	A	20010802	200239	
KR 2002013154	A	20020220	KR 200046615	A	20000811	200257	
KR 396879	B	20030902	KR 200046615	A	20000811	200412	
US 6740531	B2	20040525	US 2001923670	A	20010307	200435	

Priority Applications (No Type Date): KR 200046615 A 20000811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020021544	A1		25	H01H-047/18	
JP 2002100742	A		18	H01L-027/105	
KR 2002013154	A			H01L-027/108	
KR 396879	B			H01L-027/108	Previous Publ. patent KR 2002013154
US 6740531	B2			H01L-021/00	

Abstract (Basic): US 20020021544 A1
Abstract (Basic):
NOVELTY - An integrated circuit memory device has dielectric regions ***protected*** with multilayer insulation structures.
DETAILED DESCRIPTION - A memory device comprises:
(a) a capacitor having a lower electrode, an upper electrode, and a dielectric layer interposed between the lower electrode and the upper electrode; and
(b) a multi-layered encapsulating layer surrounding the capacitor and comprising a first blocking layer which is **annealed** and a first **protection** layer formed on the **annealed** first blocking layer. The first blocking layer and the first ***protection*** layer are formed of the same material.
INDEPENDENT CLAIMS are also included for the following:
(A) an integrated circuit comprising (i) a ferroelectric dielectric region on a substrate (10), (ii) a first **metal oxide** layer directly on a surface of the ferroelectric dielectric region, and (iii) a second **metal oxide** layer on the first **metal oxide** layer;

(B) a method of manufacturing the memory device; and
(C) a method of forming a **protective** structure for a ferroelectric dielectric region on an integrated circuit substrate, comprising (i) depositing a first **metal oxide** layer and the ferroelectric dielectric region, (ii) **annealing** the first **metal oxide** layer and the ferroelectric dielectric region, and (iii) depositing a second **metal oxide** layer on the first ***metal*** ***oxide*** layer.

USE - As integrated circuit memory device, e.g., ferroelectric random access memory (FRAM) devices.

ADVANTAGE - Degradation of capacitor dielectric layer can be reduced through the use of an encapsulating layer including a **protection** layer for **protecting** a capacitor from the diffusion of hydrogen generated during succeeding processes and a blocking layer for blocking the diffusion of hydrogen generated during the formation of the ***protection*** layer. It is not necessary to perform separate photolithography for isolating a cell area from a peripheral area after the formation of the blocking layer. A process of forming a metal contact is simple. Because the invention uses a thin blocking layer, an **annealing** process for the blocking layer is performed within a short time at 400-600 degreesC. An increase in the plug resistance of a buried contact under a capacitor can be suppressed while a memory device is being manufactured.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view illustrating an integrated circuit memory device.

Substrate (10)
Interlayer insulation layer (24)
Lower electrode (34)
Ferroelectric dielectric region (36)
Upper electrode (38)
Blocking layers (40, 48)
Protection layers (42, 50)
pp; 25 DwgNo 1a/4

18/3,AB/12 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013687875
WPI Acc No: 2001-172099/200118
XRAM Acc No: C01-051749
Catalyst for removal of odor from waste gas, involves providing catalyst layer which contains titanium **oxide**, alumina and noble **metal** catalyst to support which consists of metal base
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000300988	A	20001031	JP 99114430	A	19990422	200118	B

Priority Applications (No Type Date): JP 99114430 A 19990422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000300988	A		7	B01J-023/38	

Abstract (Basic): JP 2000300988 A

Abstract (Basic):
NOVELTY - The catalyst is set by providing a catalyst layer (5) which contains titanium oxide, alumina and catalyst of noble metals, to a catalyst support. The support consists of a base metal (3) which has a heat ***passivation*** film (3a).
DETAILED DESCRIPTION - The catalyst consists of titanium oxide and alumina as principal components. More than one type of barium, **cerium**, strontium and **oxide** of lanthanums are added as co-catalysts. A coating of slurry which contains colloidal alumina and silica or a mixture of both, is provided to the base metal. An INDEPENDENT CLAIM is also included for catalyst manufacturing method.
USE - For removing odor from waste gas, chlorine gas.
ADVANTAGE - Provides highly durable catalyst object with strong adhesion of catalyst layer and excelled purification capability, as the catalyst layer formed with titanium oxide, alumina is provided on metal base having heat ***passivation*** film. Offers highly corrosion-resistant catalyst object by carrying out heat ***annealing*** of catalyst by combustion in exhaust gas.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of the composition of catalyst object.
Base metal (3)
Heat **passivation** film (3a)
Catalyst layer (5)
pp; 7 DwgNo 2/3

18/3,AB/13 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013662054
WPI Acc No: 2001-146266/200115
XRAM Acc No: C01-043177
XRPX Acc No: N01-107015
Fabrication of fluorescent lamp by applying a liquid precursor solution comprising metal organic compound to a lamp wall to form a **metal oxide** thin film containing the metal
Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE); SYMETRIX CORP (SYME-N)
Inventor: BACON J W; CELINSKA J; CUCHIARO J D; KANO G; MATSUDA A; MCMILLAN L D; MORITA T; NAGAI H; PAZ DE ARAUJO C A; YAMAGUCHI Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6174213	B1	20010116	US 99388038	A	19990901	200115	B

Priority Applications (No Type Date): US 99388038 A 19990901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6174213	B1		14	B05D-007/22	

Abstract (Basic): US 6174213 B1
Abstract (Basic):
NOVELTY - A fluorescent lamp is fabricated by applying a liquid precursor solution comprising metal organic compound to a lamp wall to form a ***metal*** ***oxide*** thin film containing the metal. The metal organic compound is alkoxycarboxylates, alkoxides, ethylhexanoates, octanoates, or neodecanoates.

DETAILED DESCRIPTION - Fabrication of fluorescent lamp involves providing partially fabricated lamp having lamp envelope and a lamp wall. A liquid precursor solution comprising metal organic compound is provided. The liquid precursor solution is applied to the to the lamp wall to form a ***metal*** ***oxide*** thin film containing the metal. The fabrication of the lamp is completed to include the **metal** ***oxide*** thin film as part of the lamp wall. The metal organic compound is alkoxycarboxylates, alkoxides, ethylhexanoates, octanoates, or neodecanoates.

USE - For fabricating fluorescent lamp.

ADVANTAGE - The invention allows fine control of the manufacturing process since their composition can be easily controlled and varied, if necessary. They can be safely stored for long periods, up to six months. They are nontoxic and nonvolatile compared to precursors of prior art. The formed ***metal*** ***oxide*** thin film layers have smooth, continuous and uniform surfaces. They can be reliably fabricated to have thickness of 20-500 nm, maintaining important characteristics such as transparency and desired electrical properties.

pp; 14 DwgNo 0/6